Per-Thread Compositional Compilation for Confidentiality-Preserving Concurrent Programs

Robert Sison

13 Jan 2018

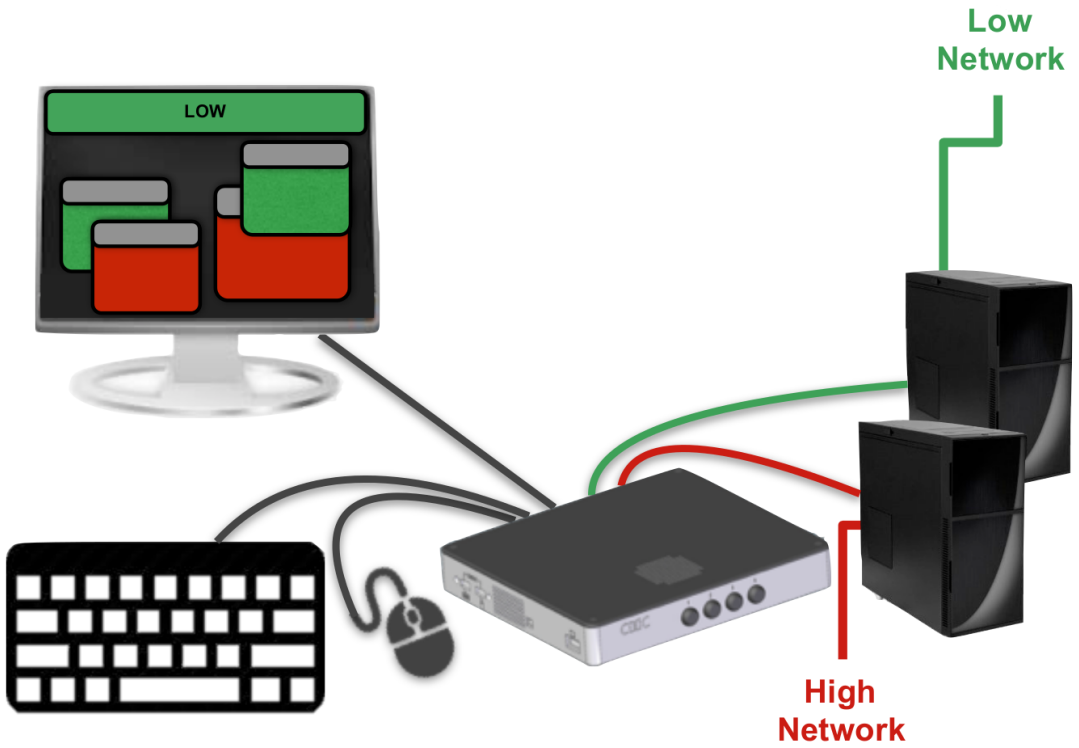
THE UNIVERSITY OF NEW SOUTH WALES

CSIRO

www.data61.csiro.au

A confidentiality-preserving program

Cross Domain Desktop Compositor (CDDC)
[Beaumont et al, 2016]



Data61/DSTG project for de-duplicating user-facing hardware.

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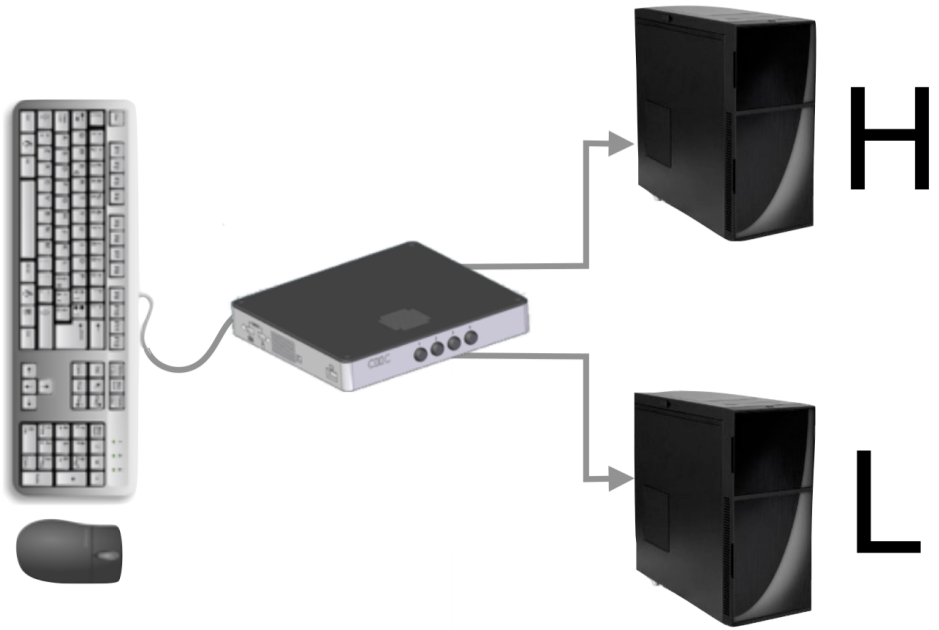

Challenge #1: value-dependent security classifications

A confidentiality-preserving program

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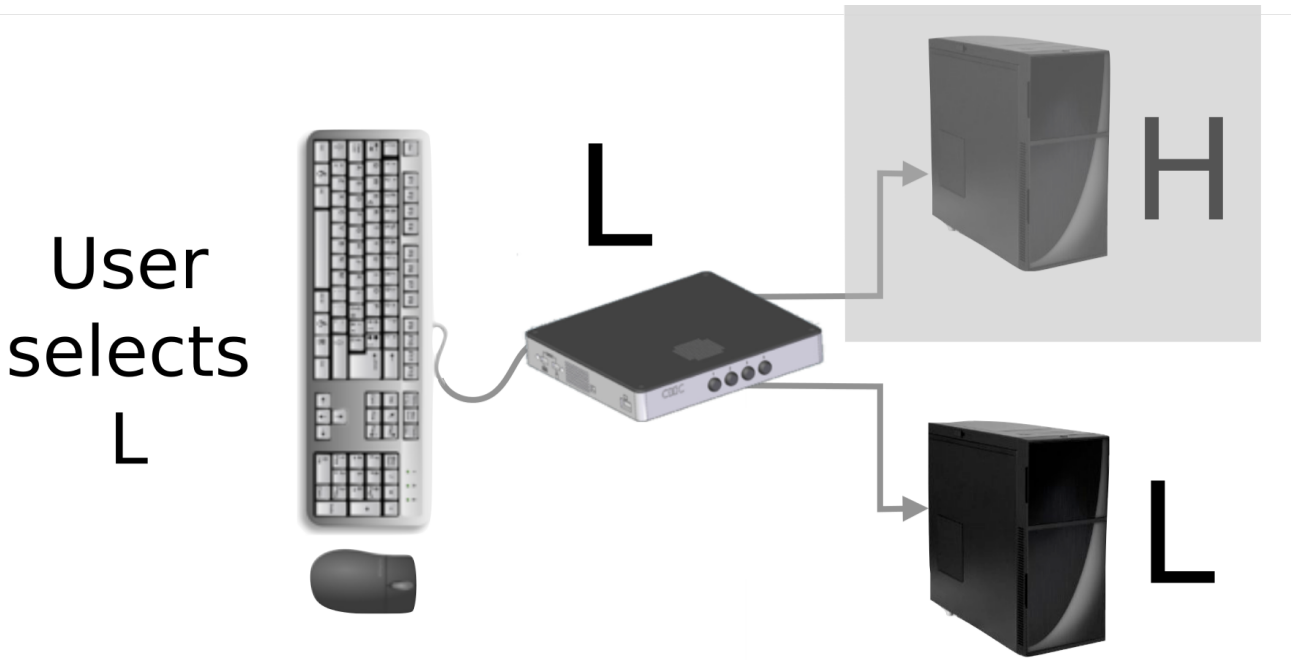

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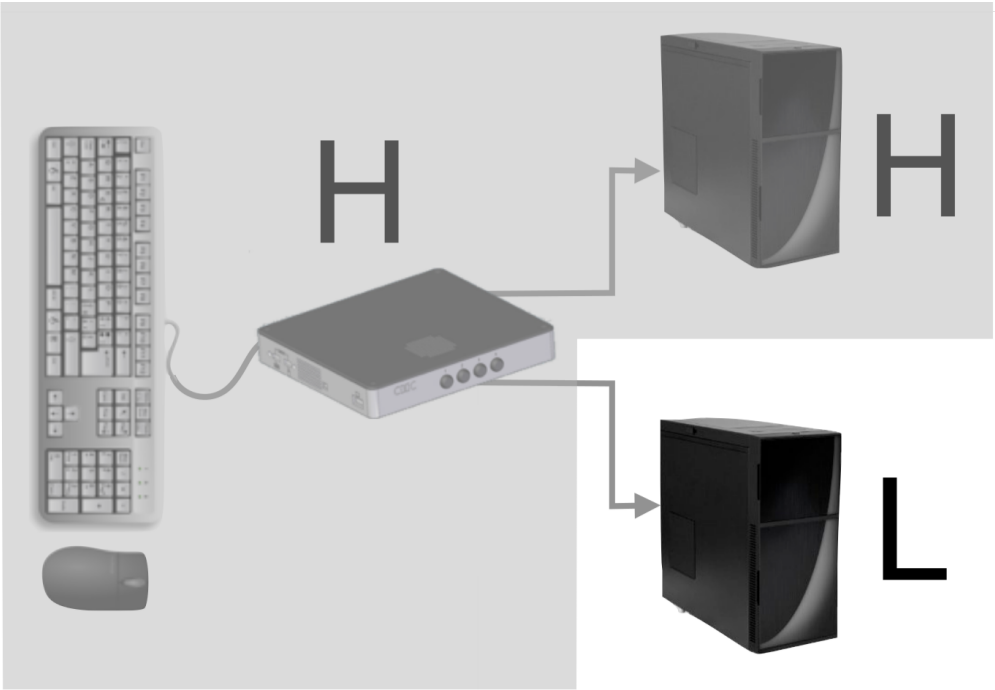
User selects H



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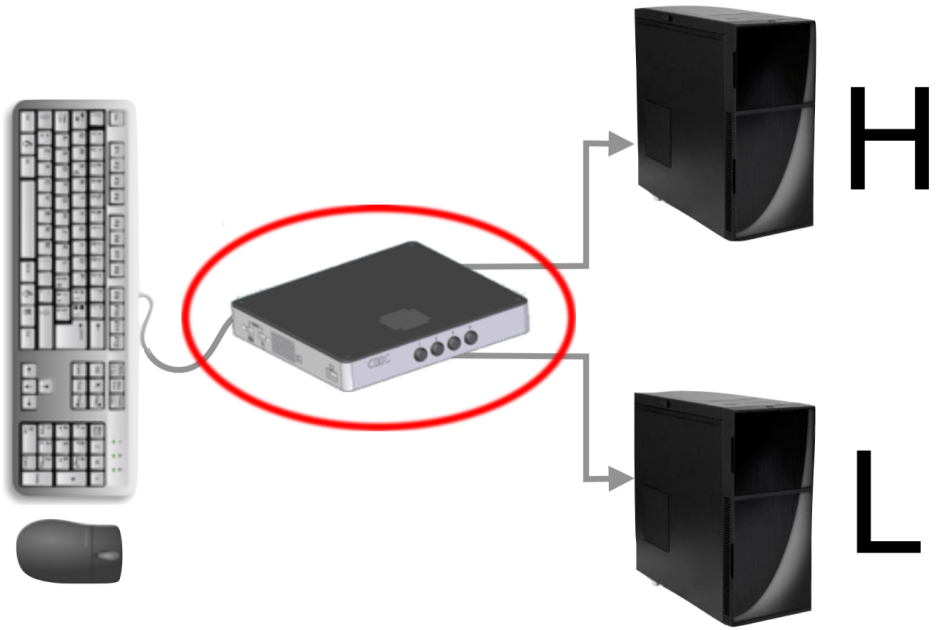
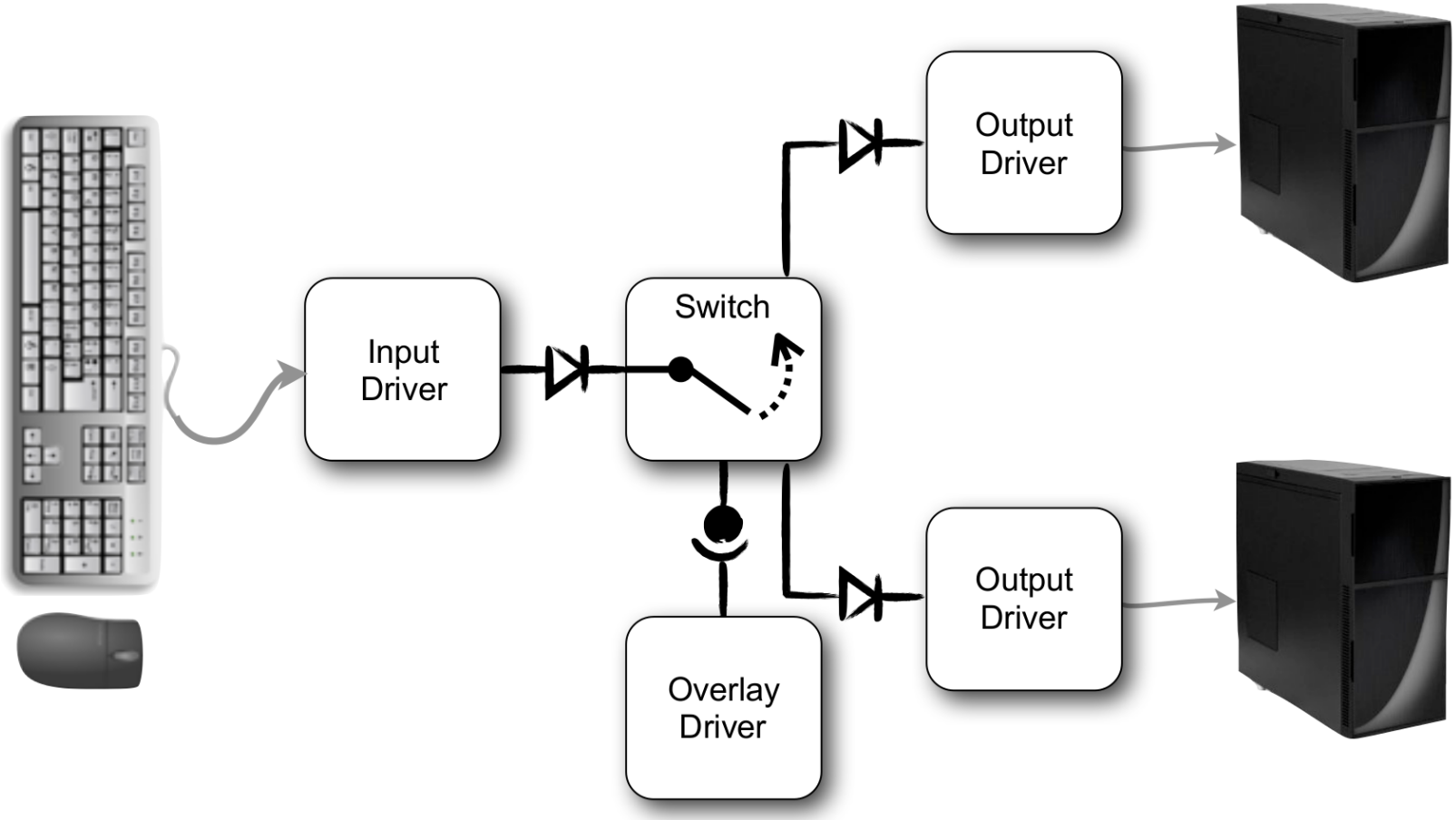


Challenge #2: shared-variable concurrency

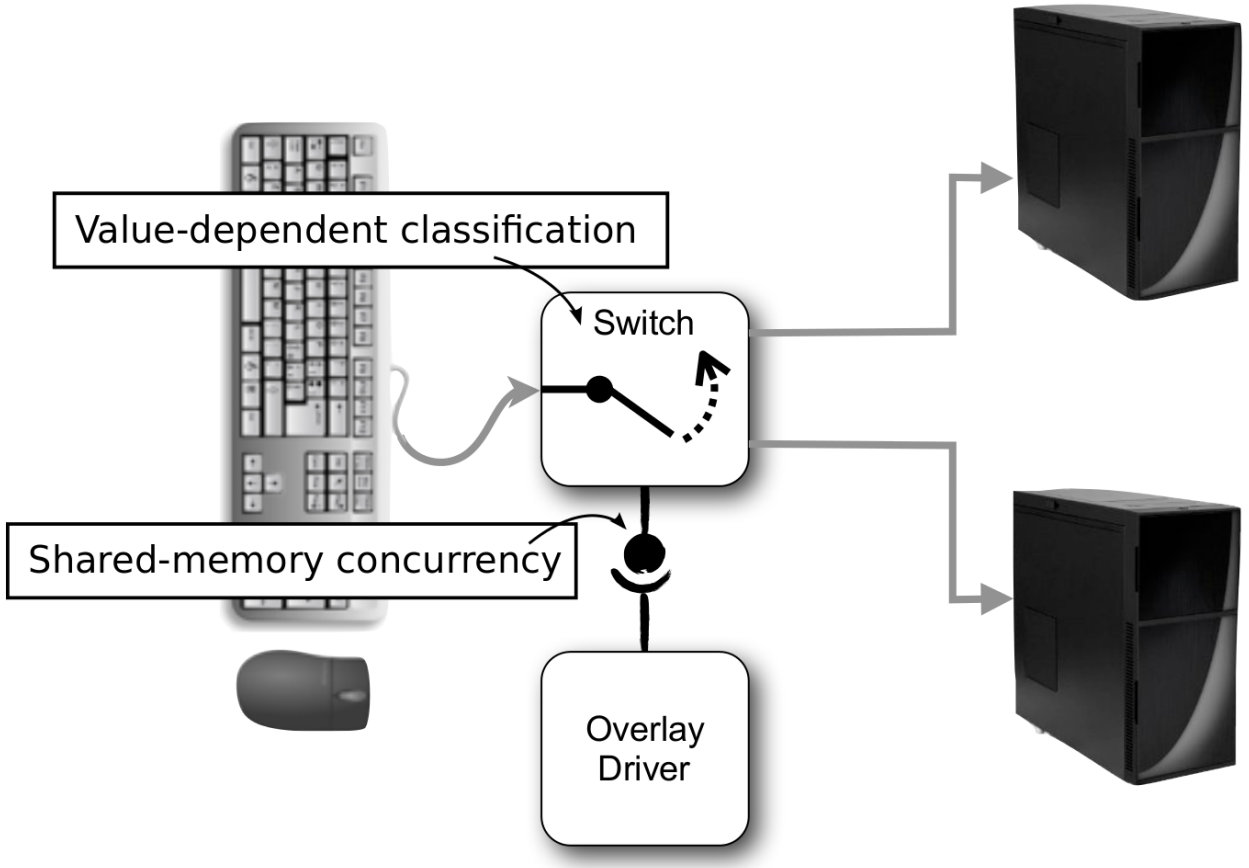
A confidentiality-preserving concurrent program

CDDC seL4-based software architecture:



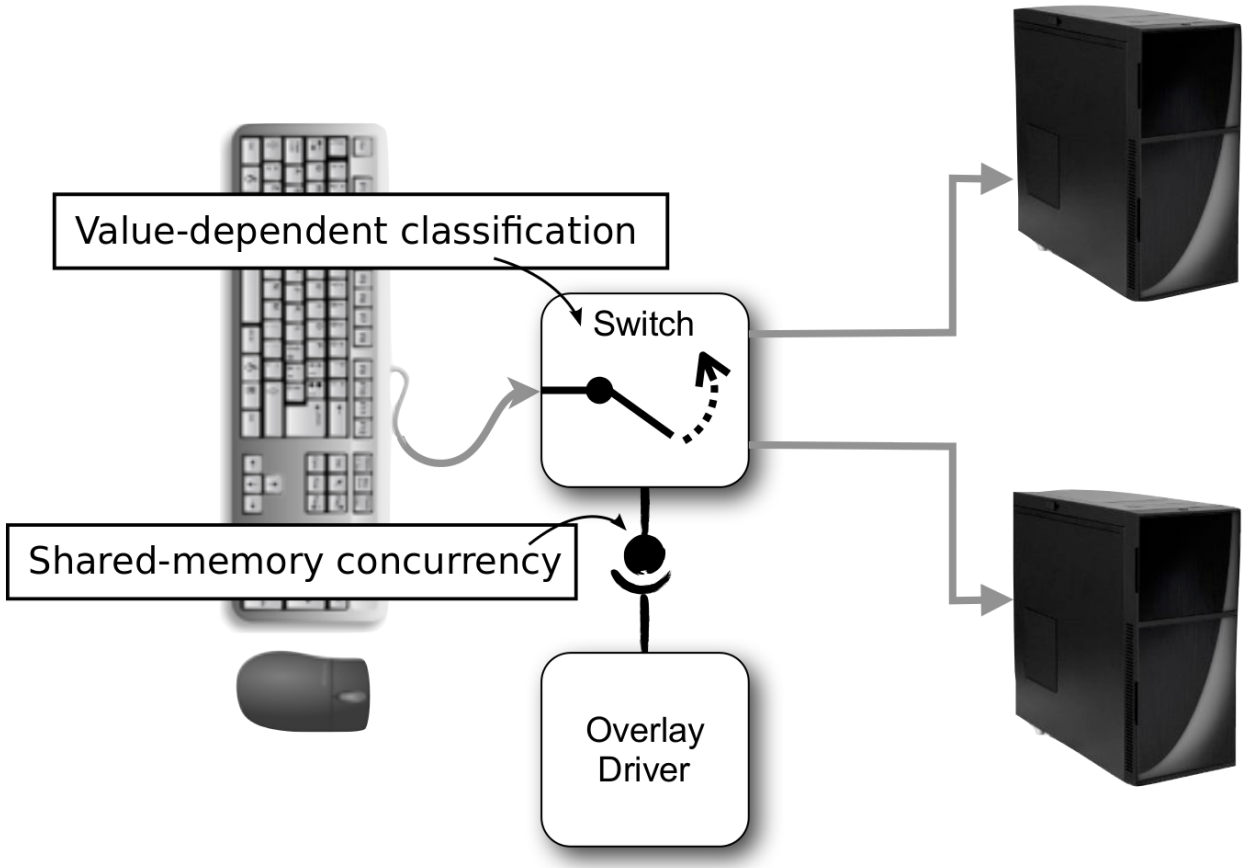
A confidentiality-preserving concurrent program

CDDC seL4-based software architecture (simplified model):



Per-thread compositional verification

Challenge #3: per-thread compositionality of proofs



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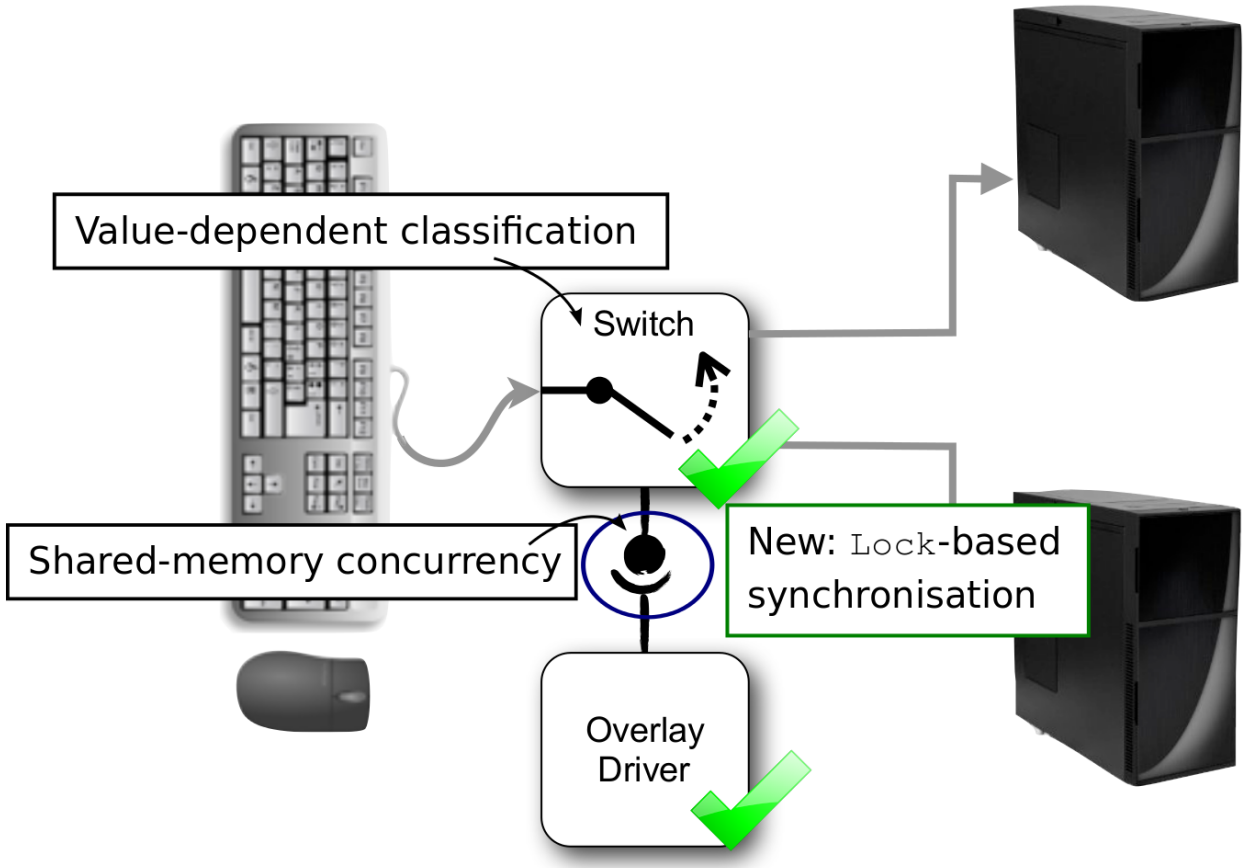

Mechanized in Isabelle/HOL. (More to appear: EuroS&P'18.)

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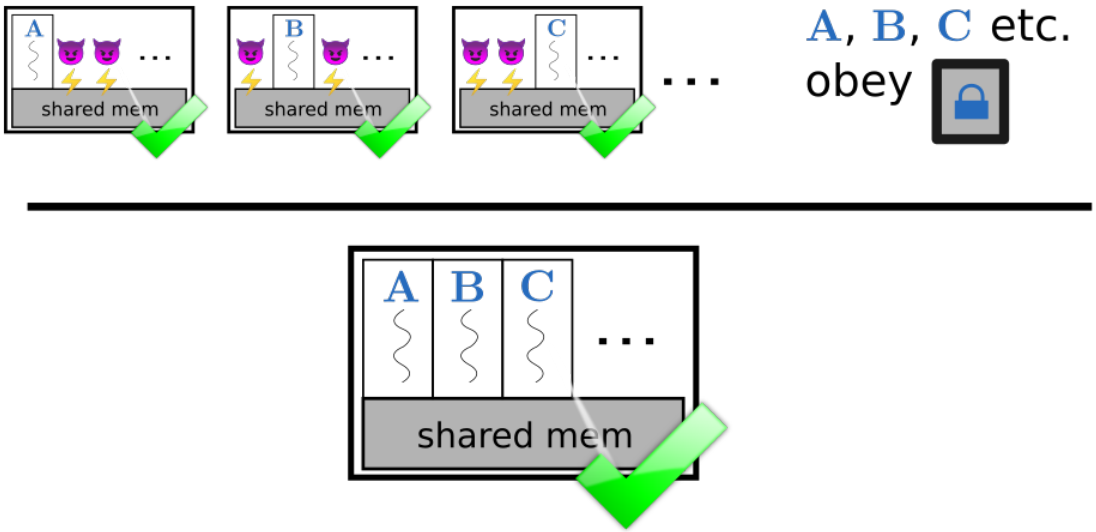
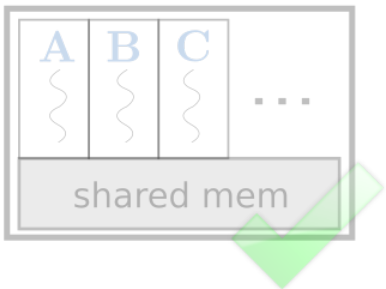


Per-thread compositional compilation

Challenge #3: per-thread compositionality of proofs

A, B, C etc. obey

Source



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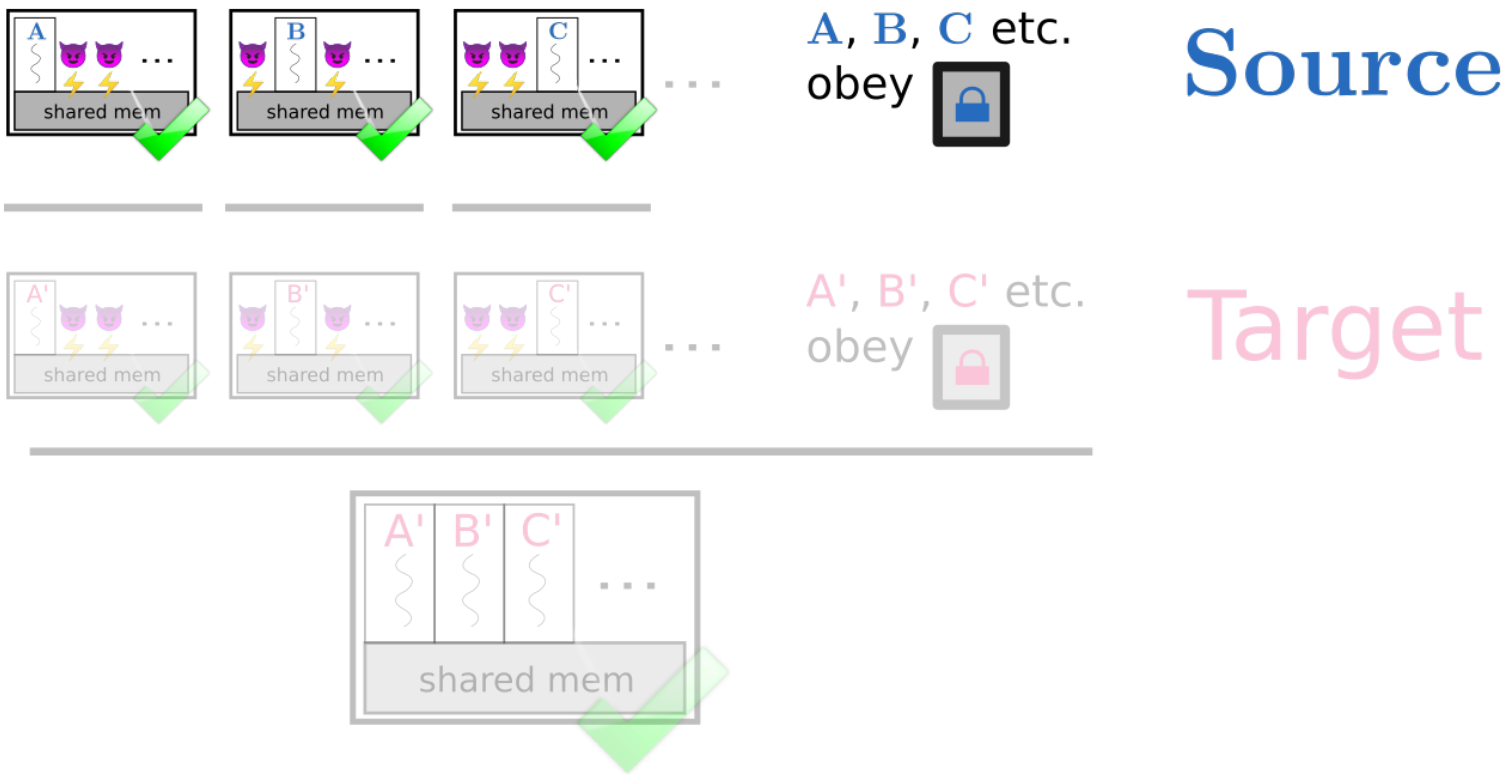

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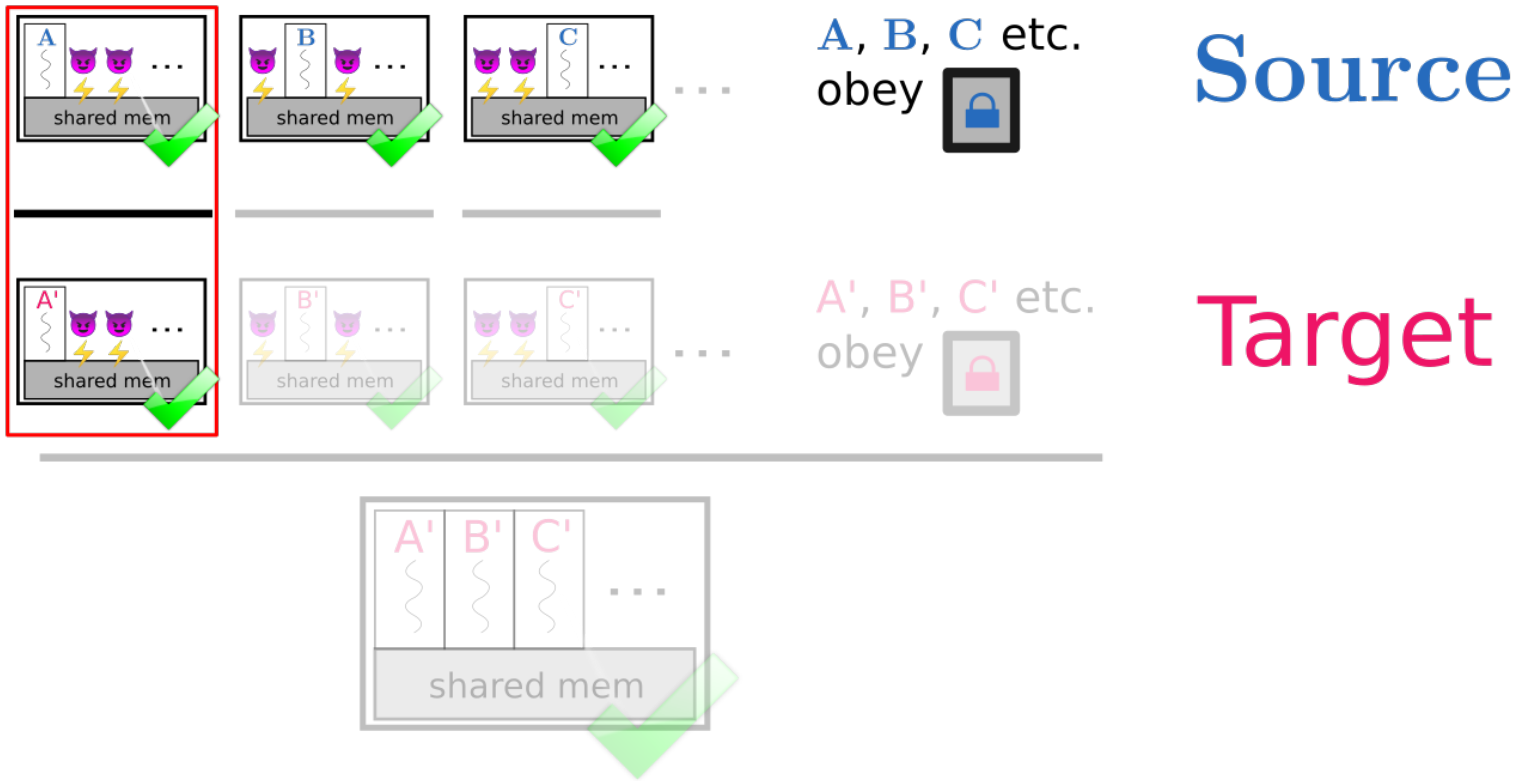

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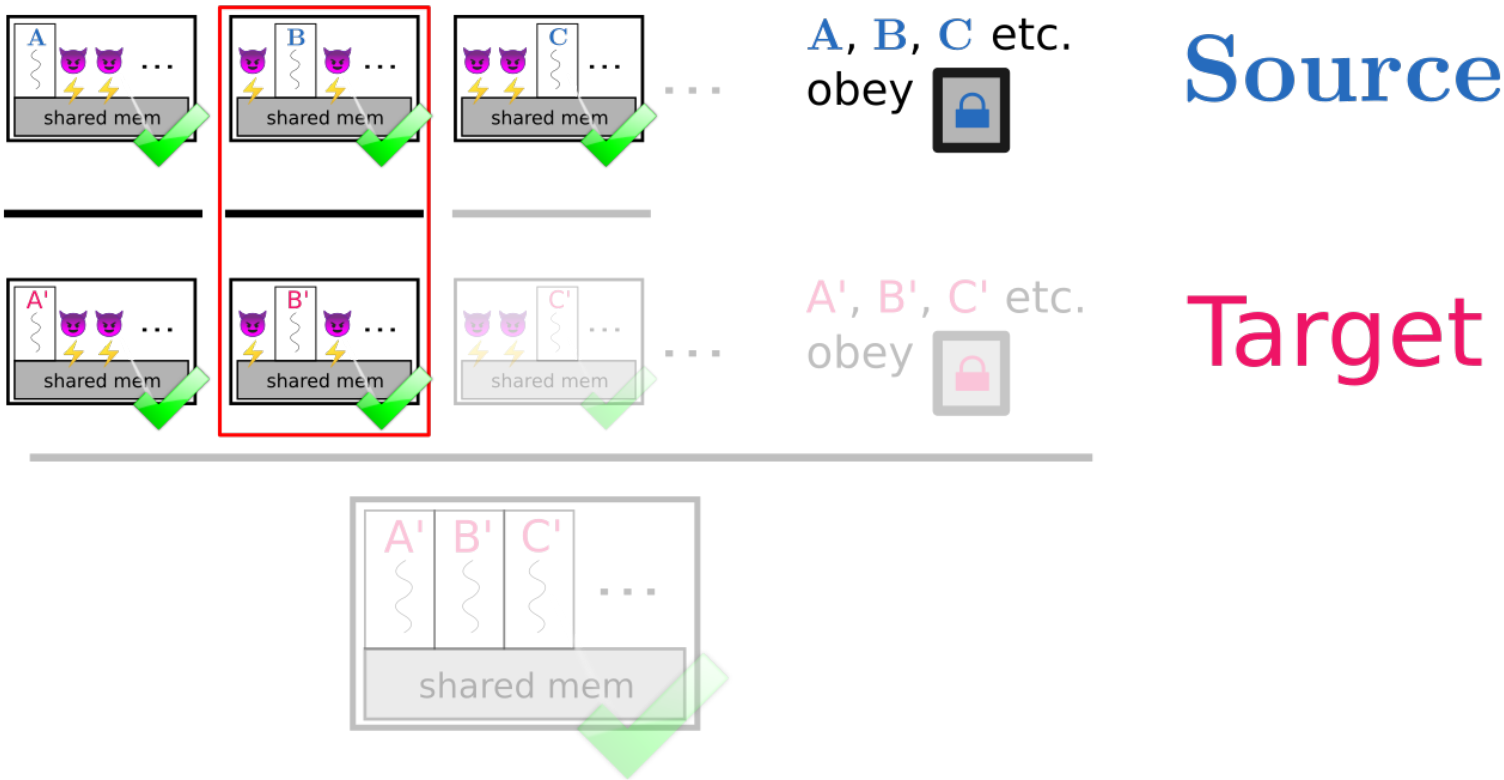

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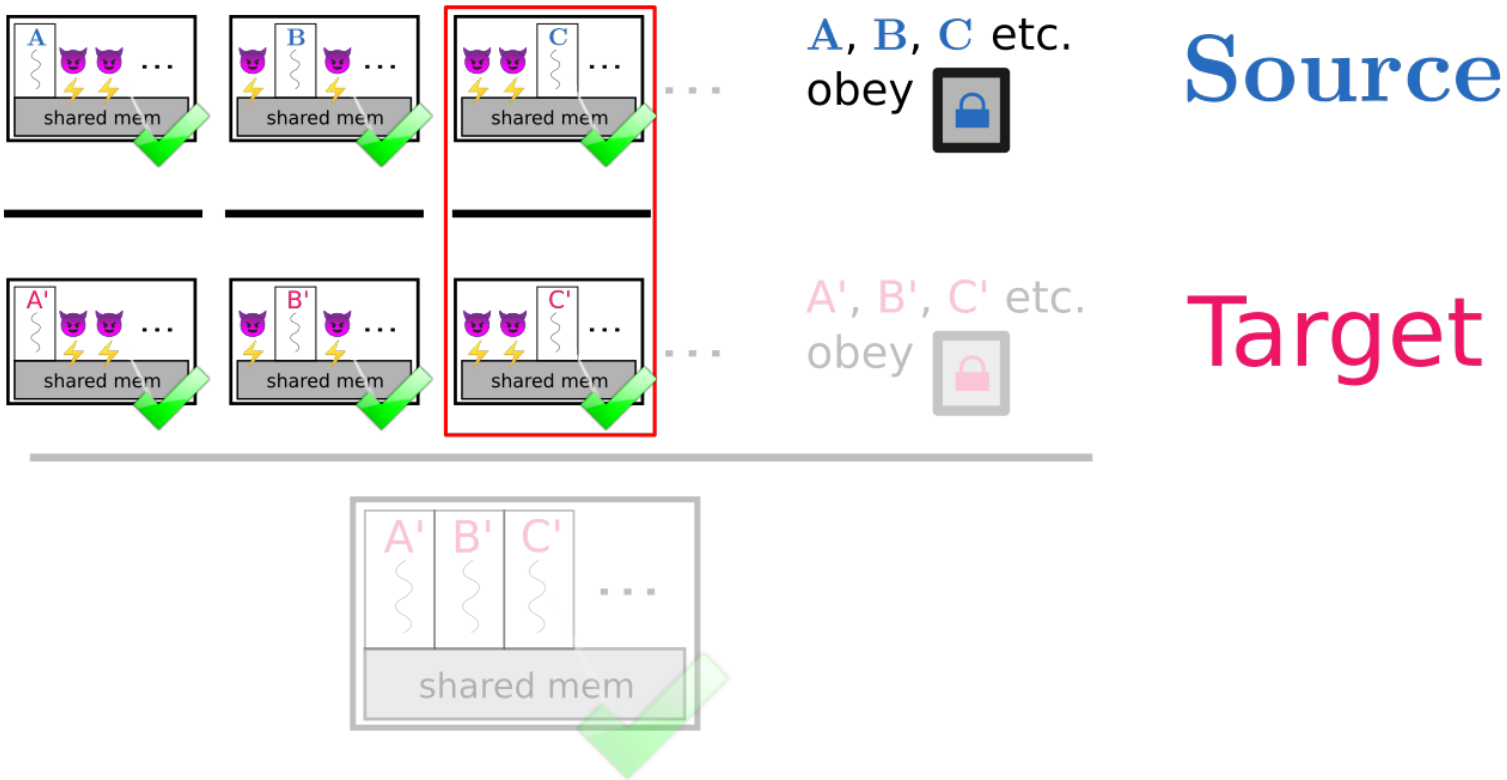

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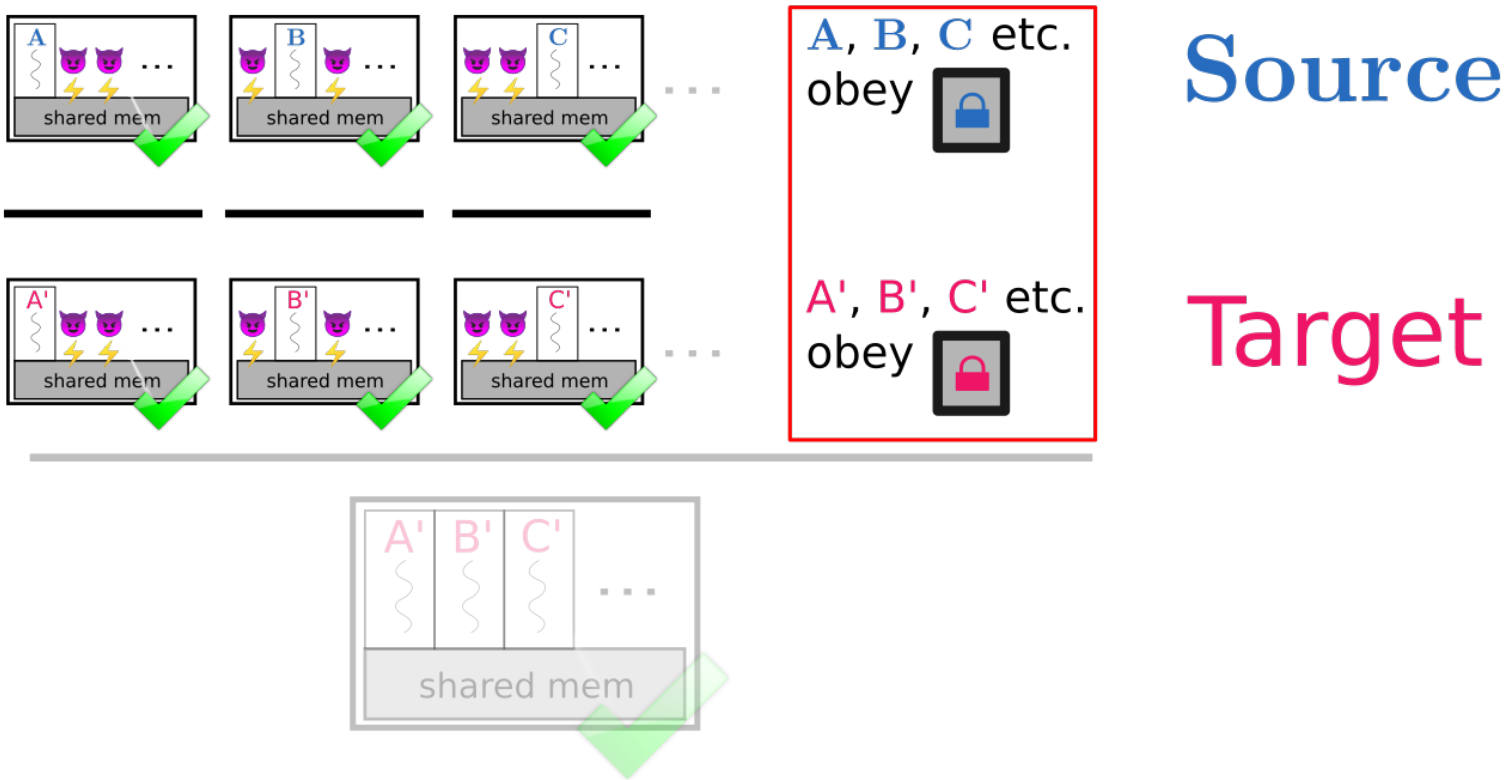

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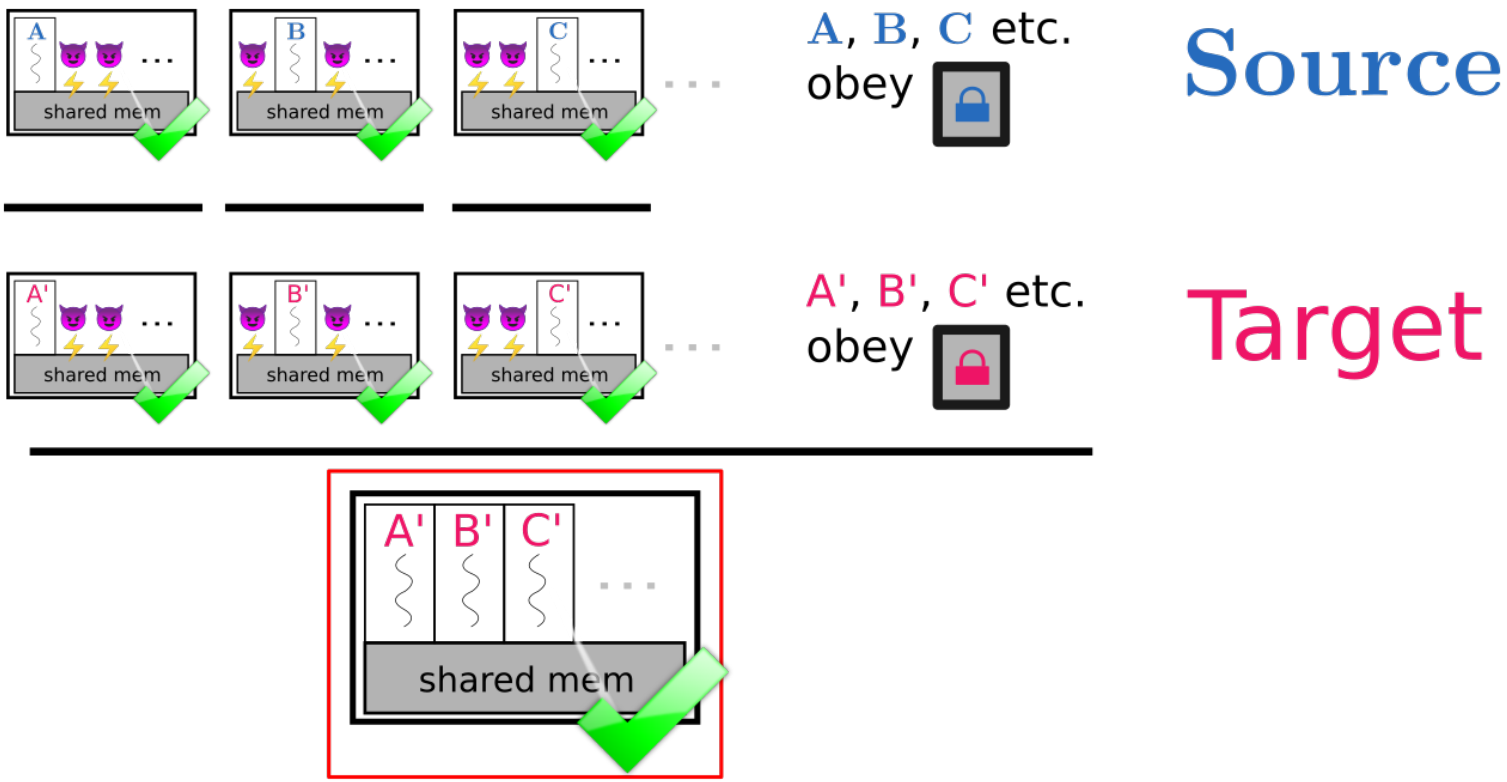
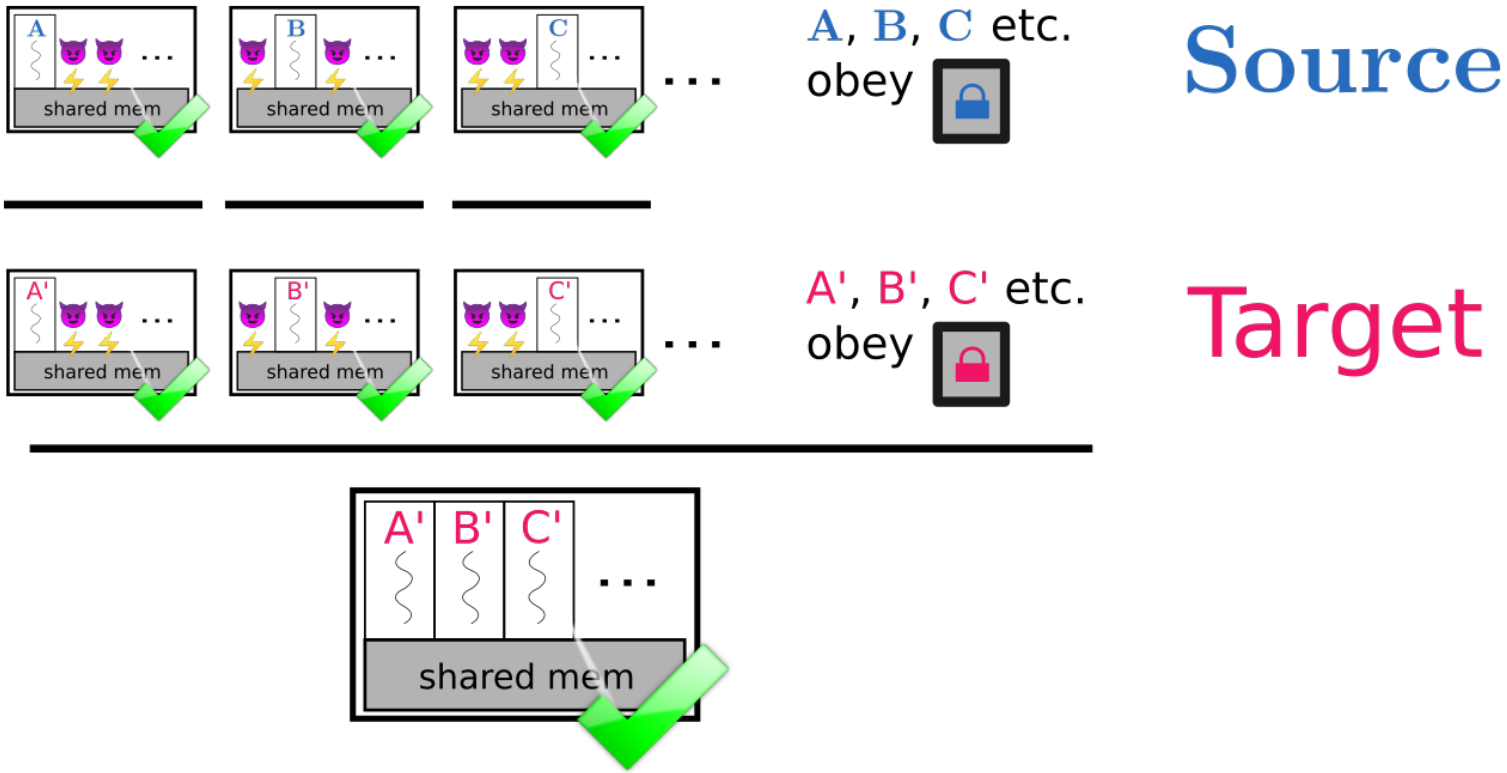


This talk

Part 1: Concurrent value-dependent noninterference
Part 2: Per-thread compositional refinement
Part 3: While-to-RISC compiler verification



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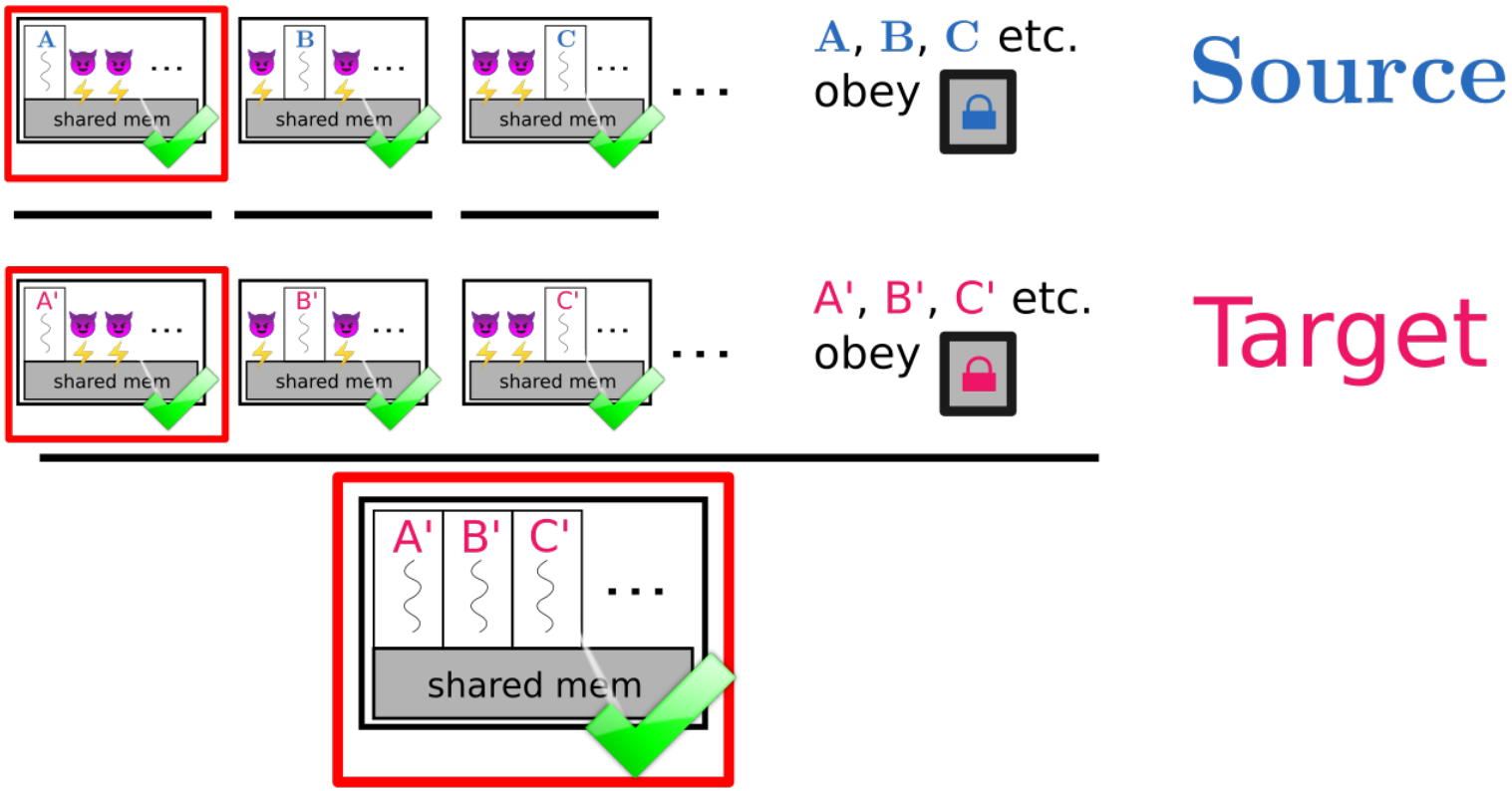

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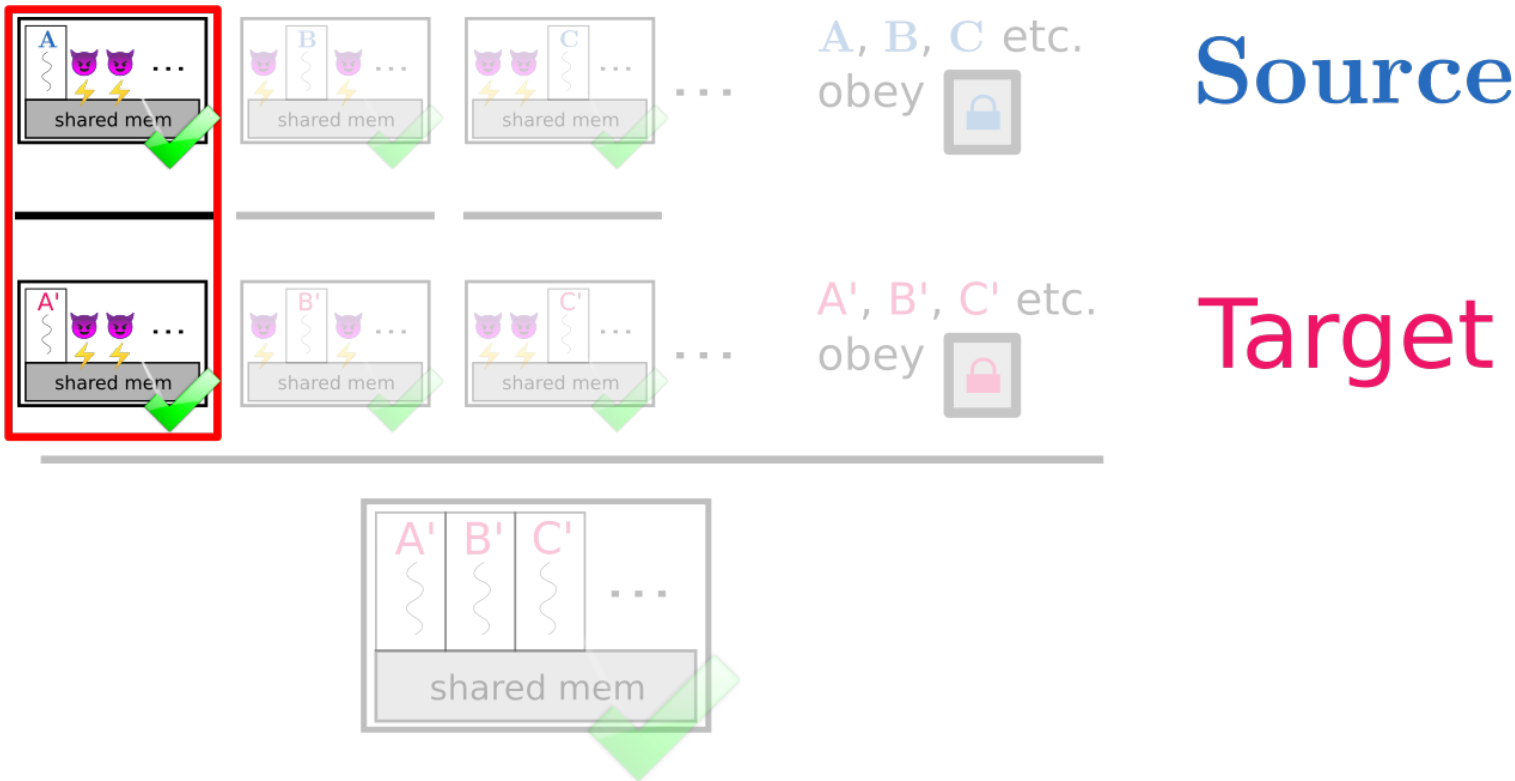

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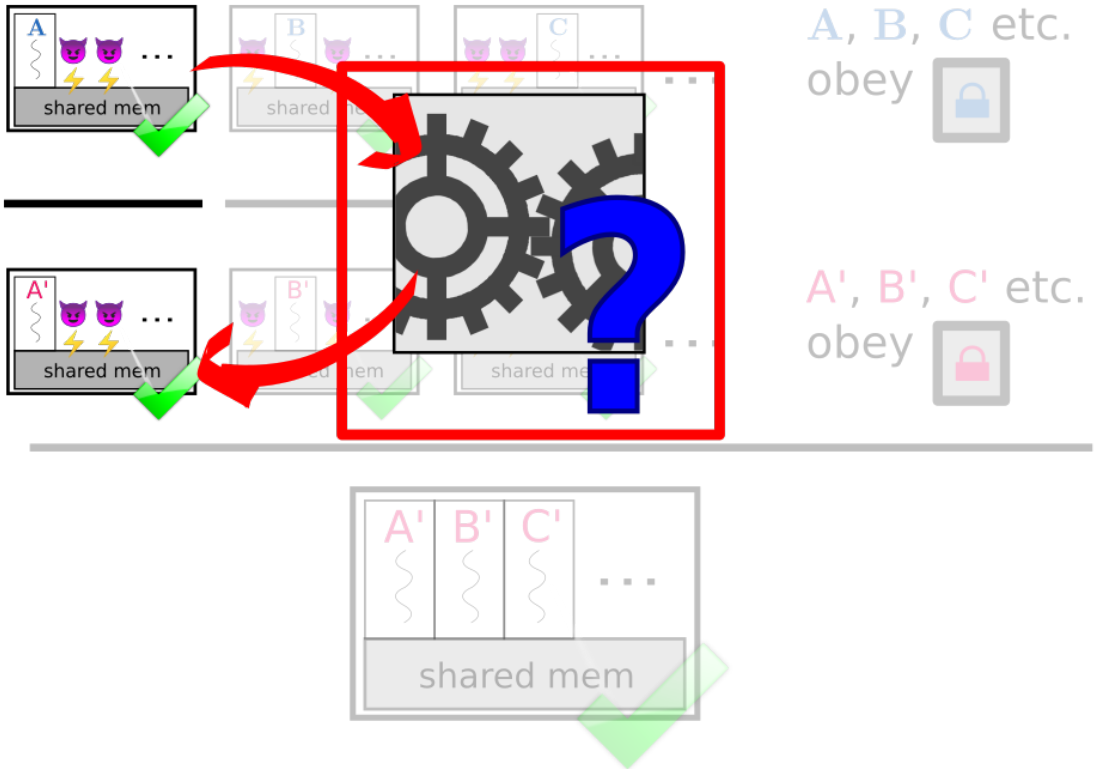

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obey

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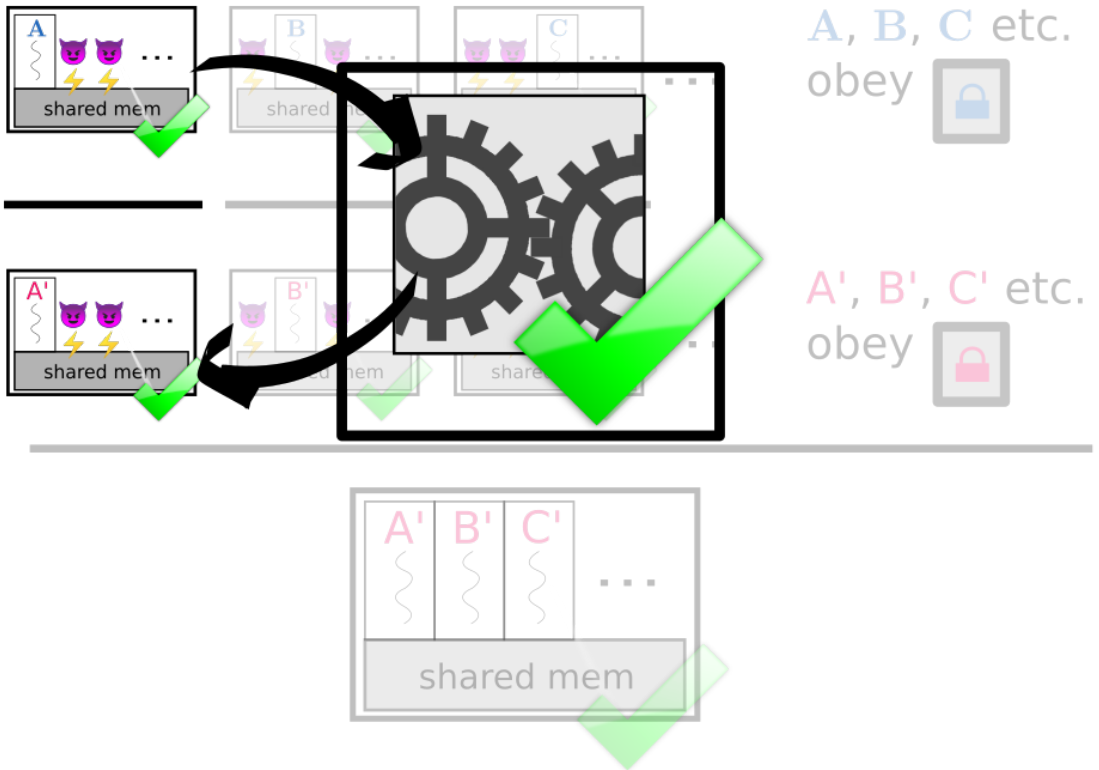

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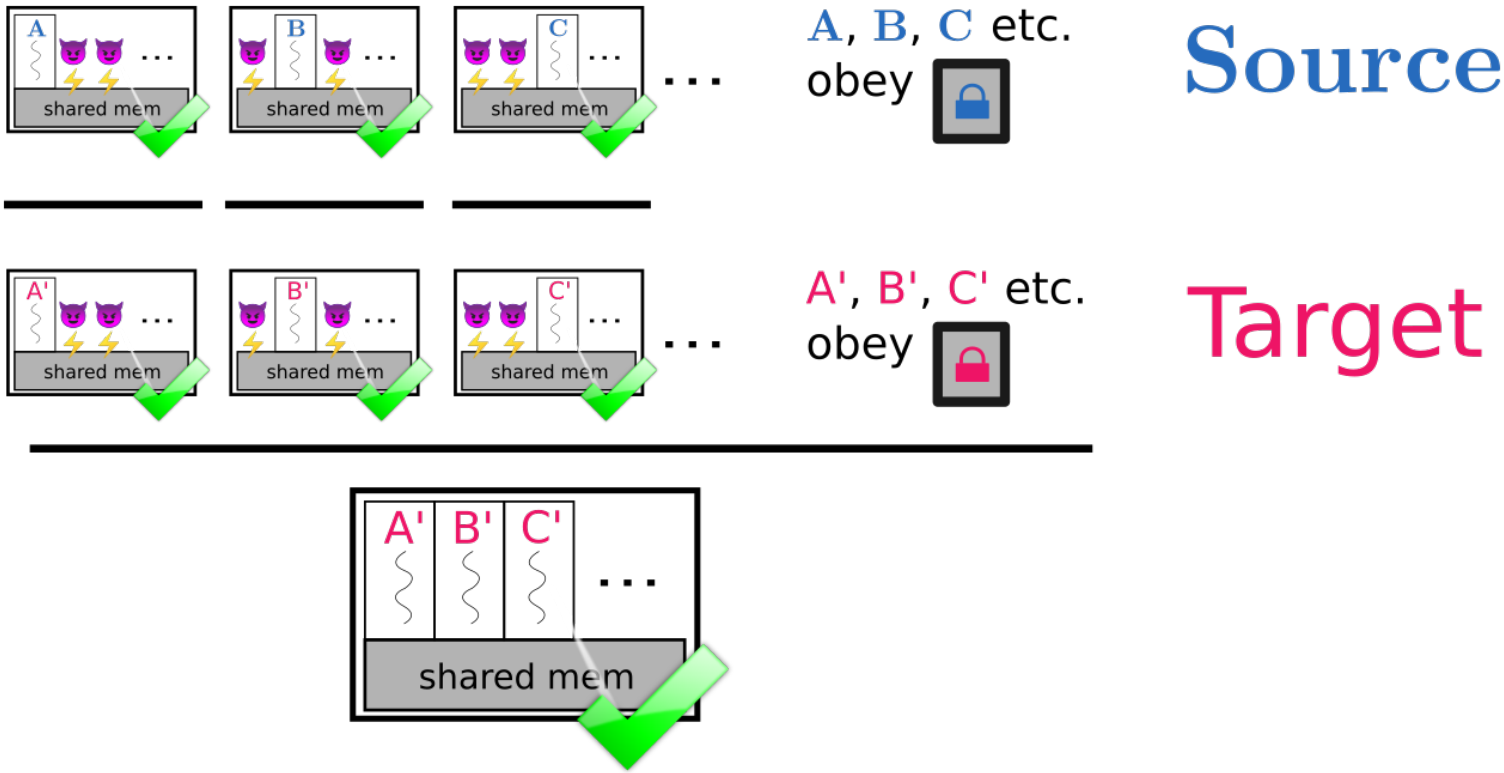

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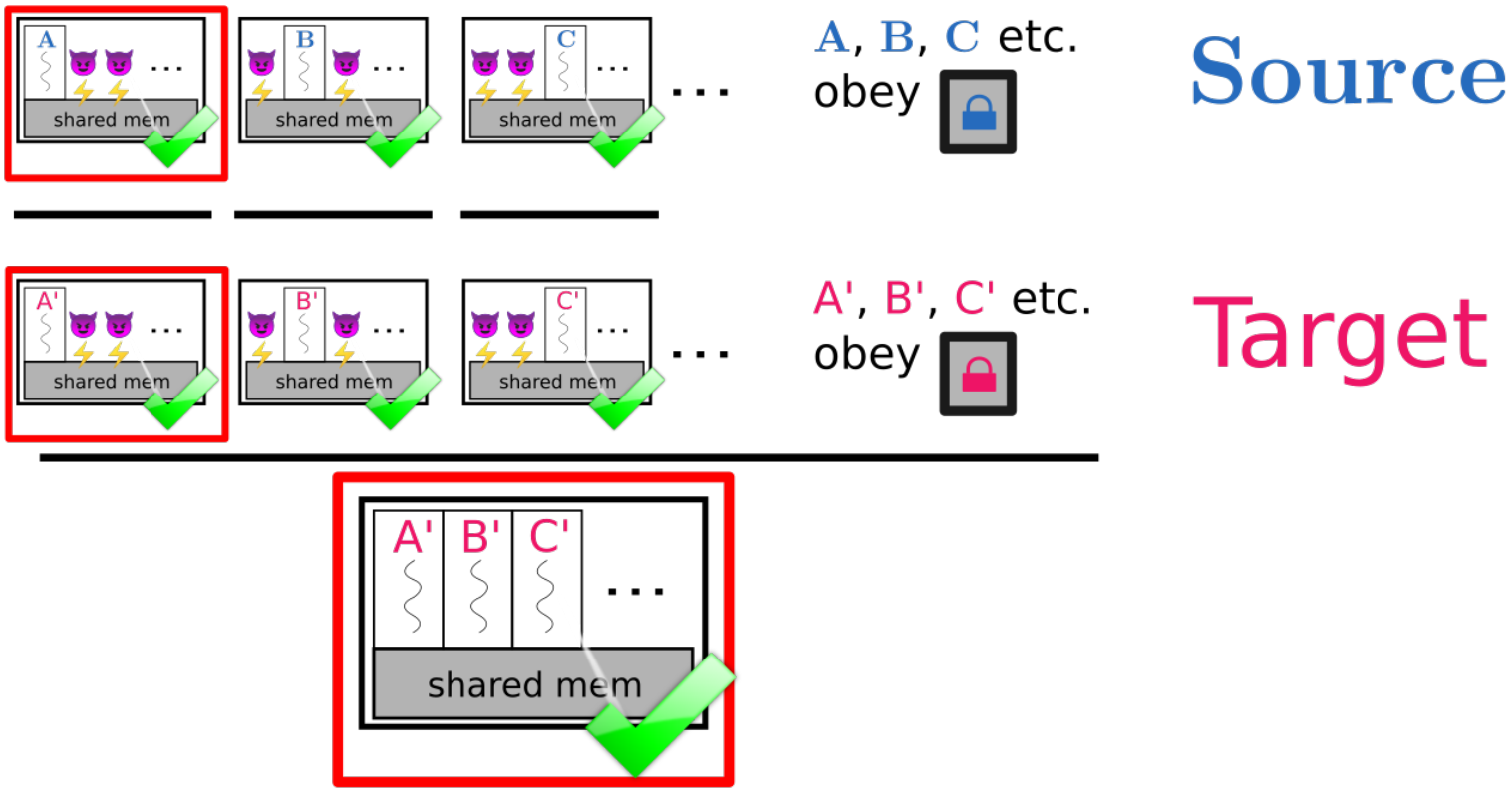

The confidentiality property

Concurrent value-dependent noninterference.

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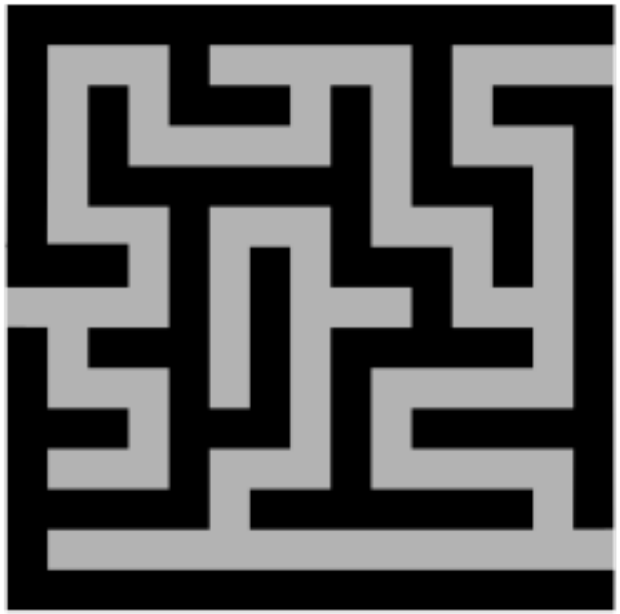
Simplest policy: **H**igh $\not\rightarrow$ **L**ow

Low part of state must remain indistinguishable.



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Reflects the *attacker model*.

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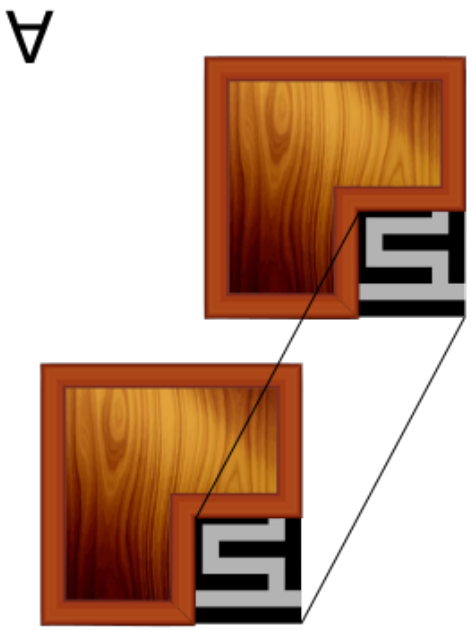

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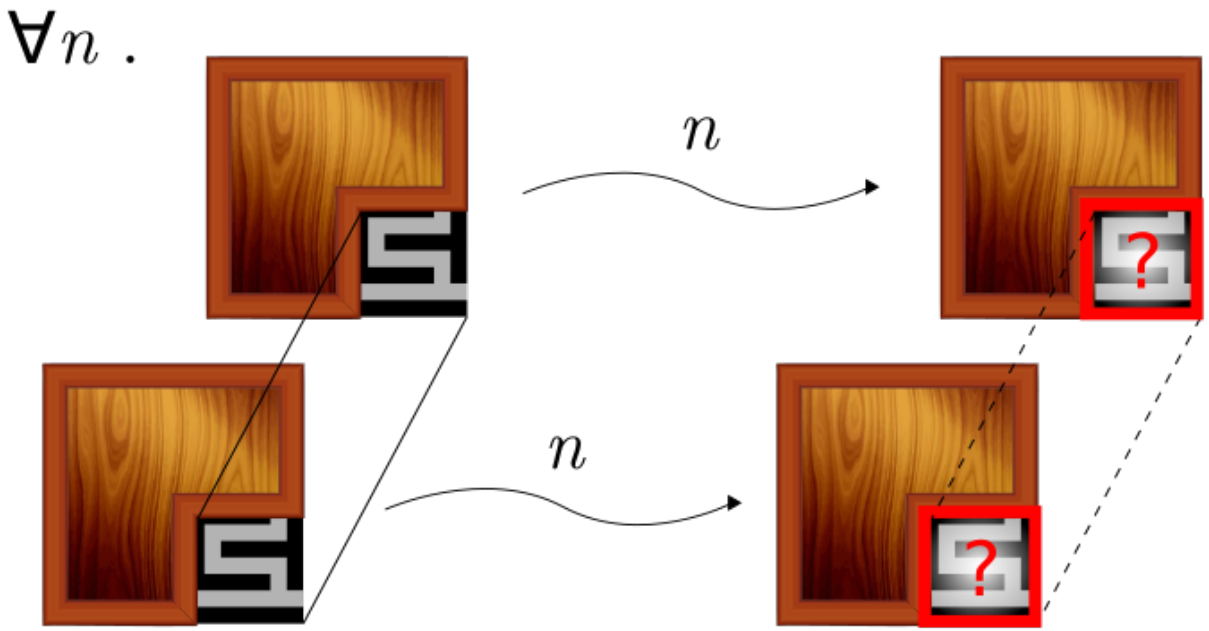

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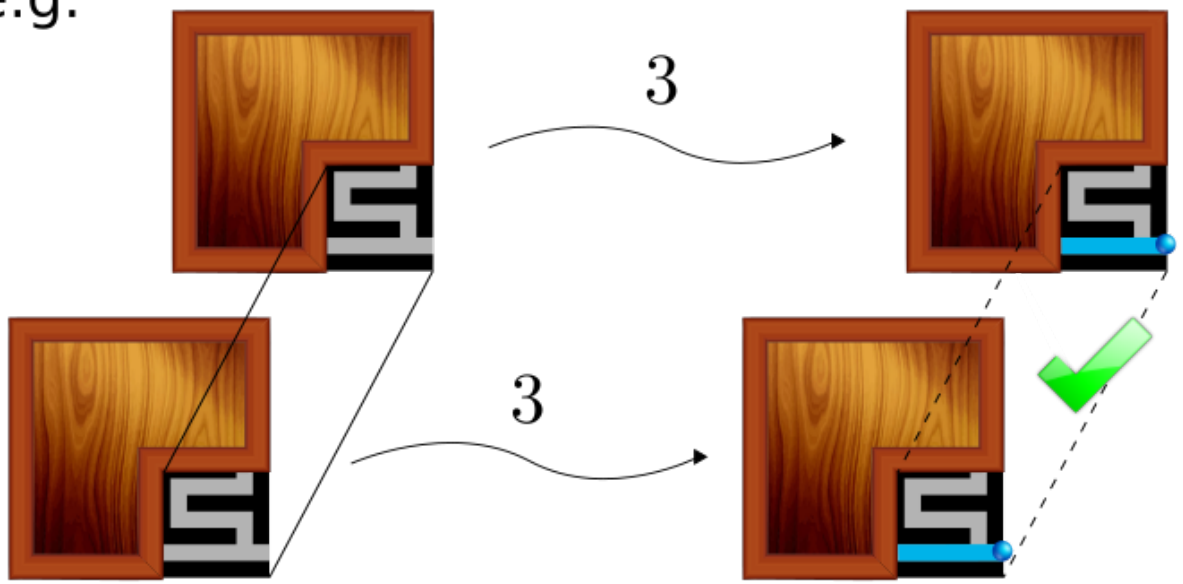

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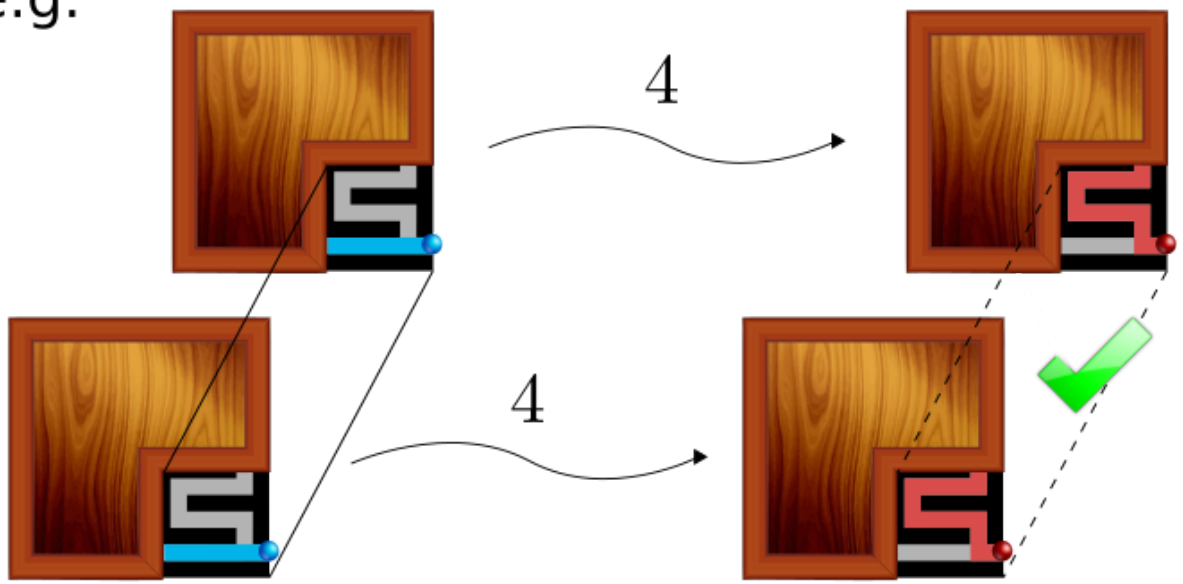

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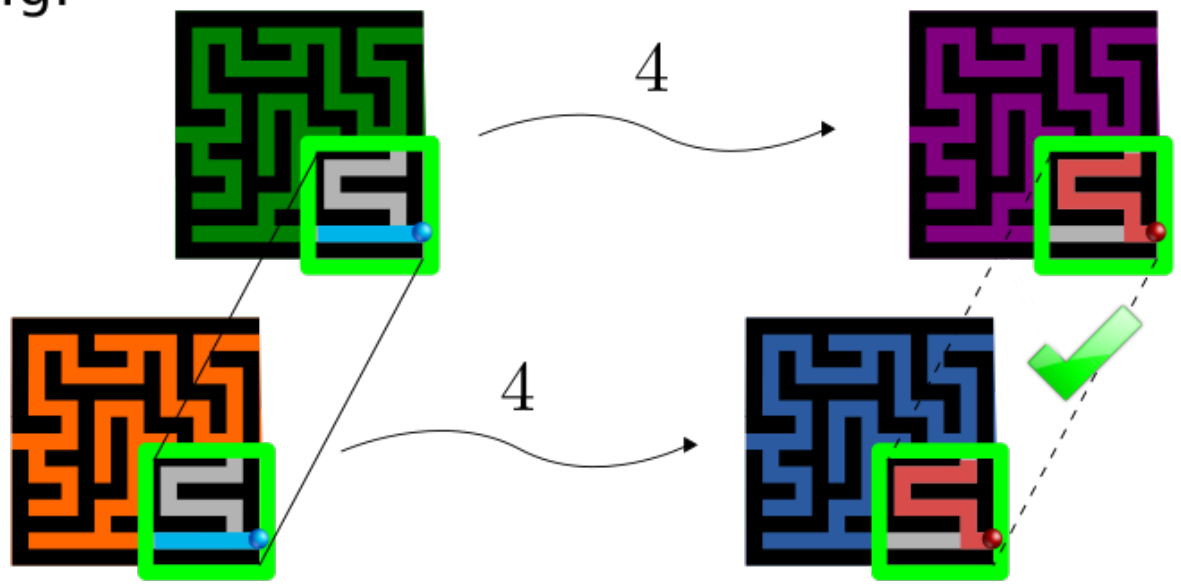

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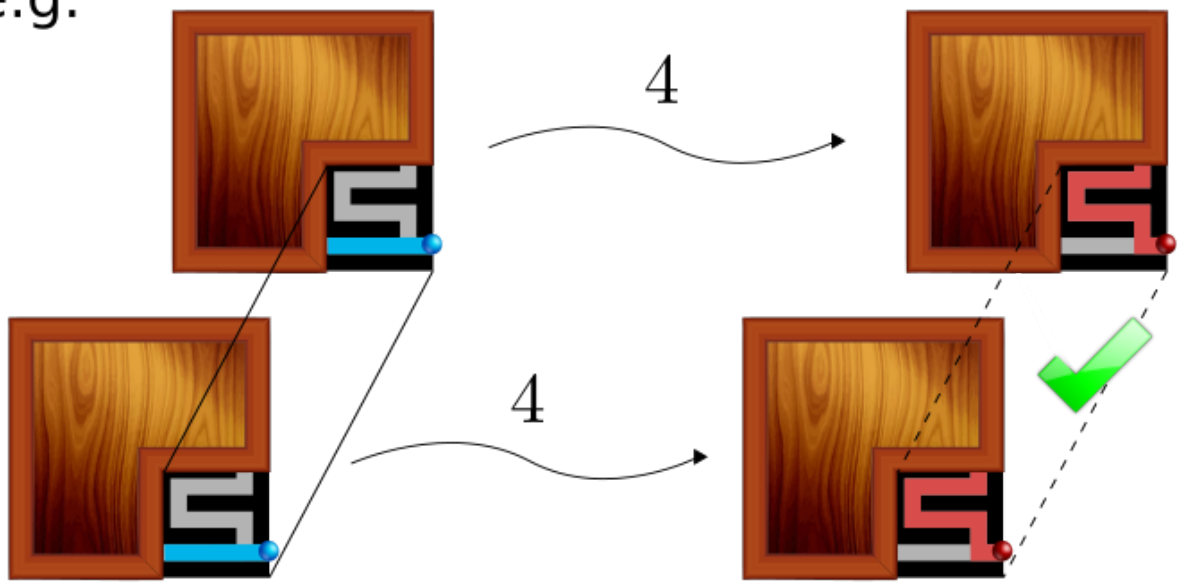

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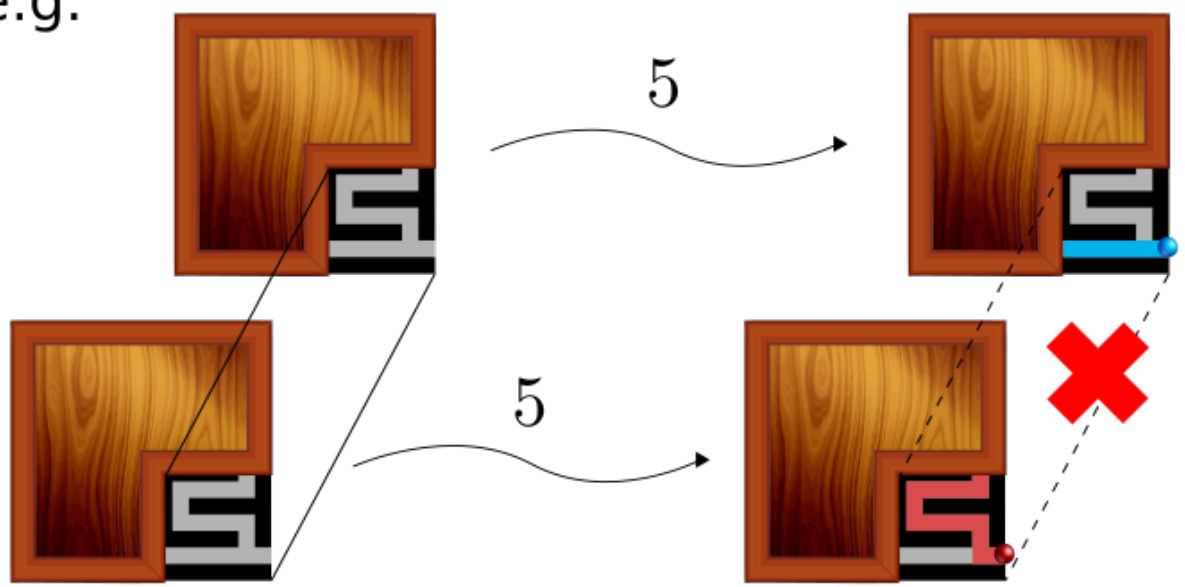

- A 2-safety hyperproperty.

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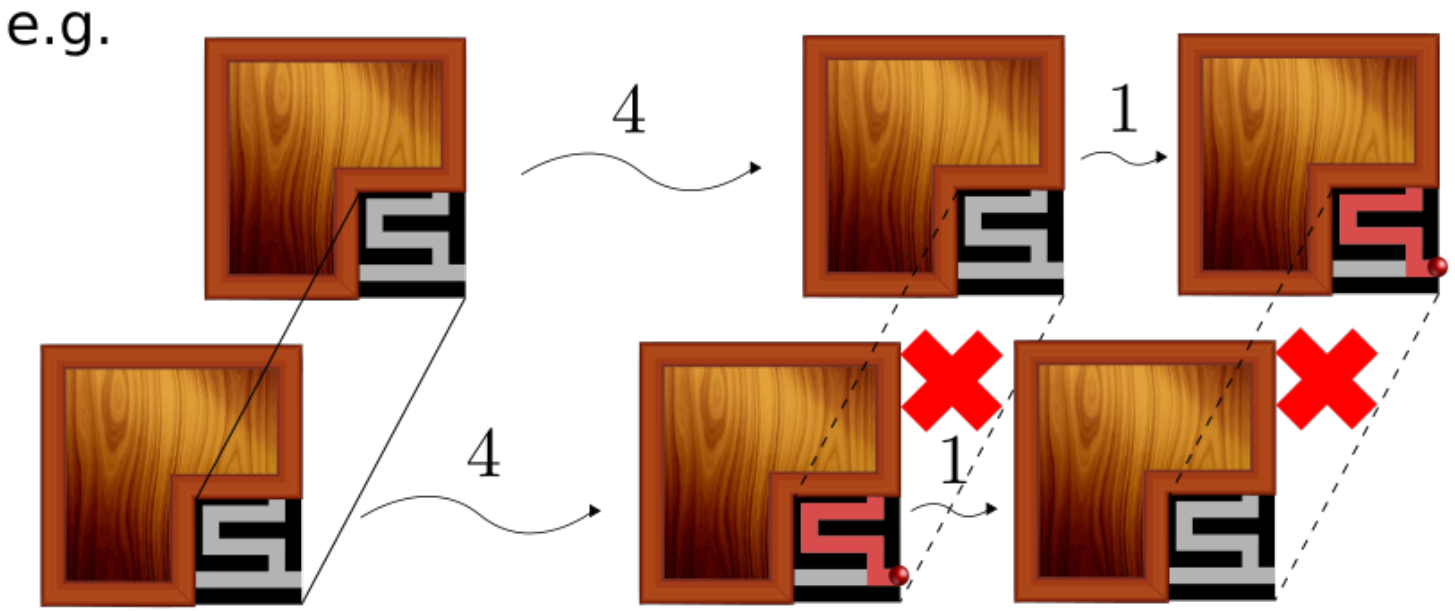

- A 2-safety hyperproperty.
- Timing-sensitive. (Want this for concurrency reasons.)

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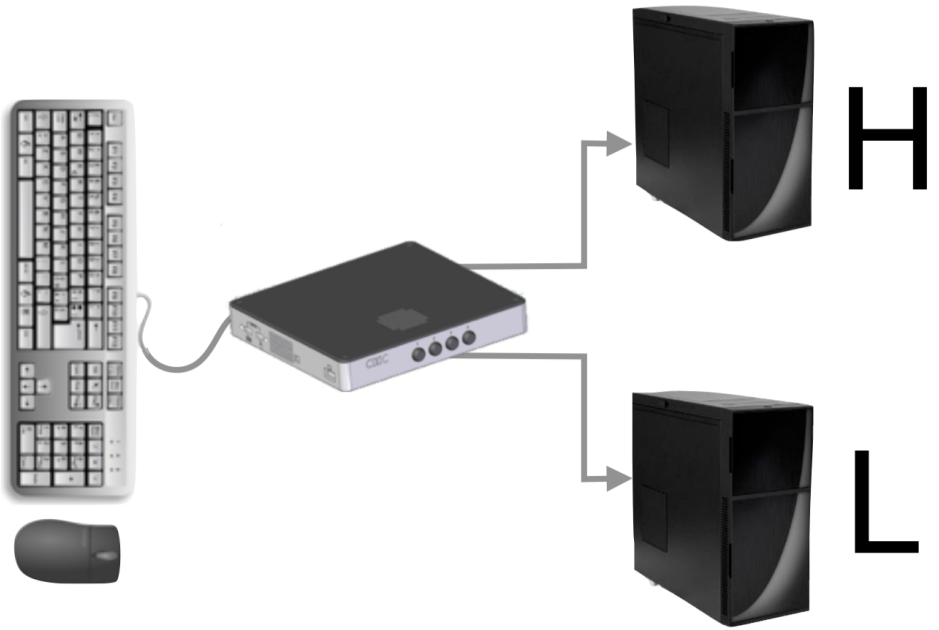

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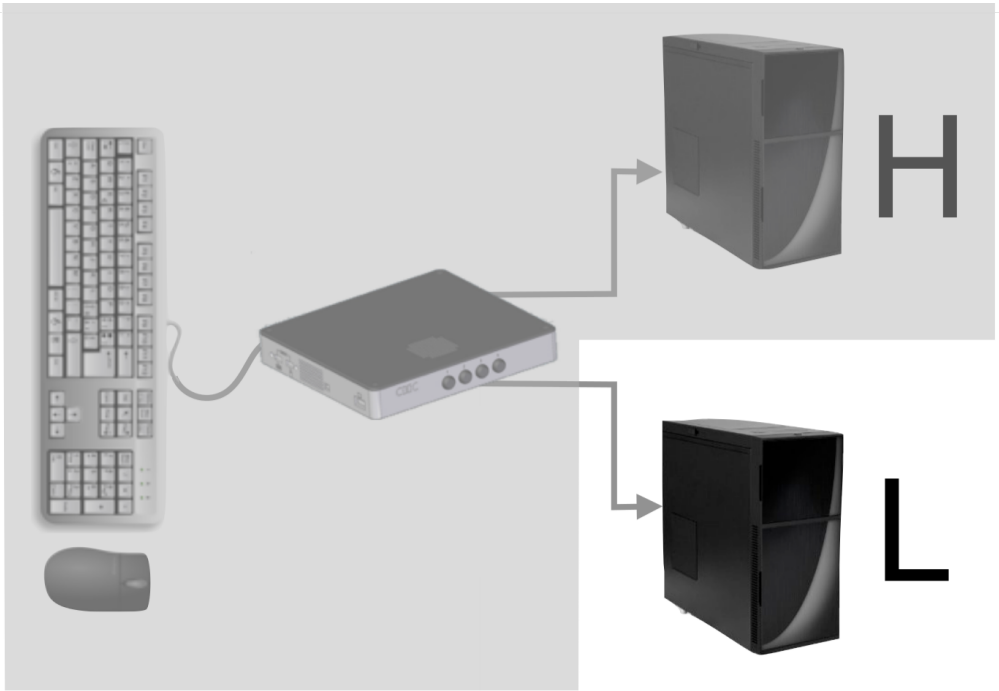

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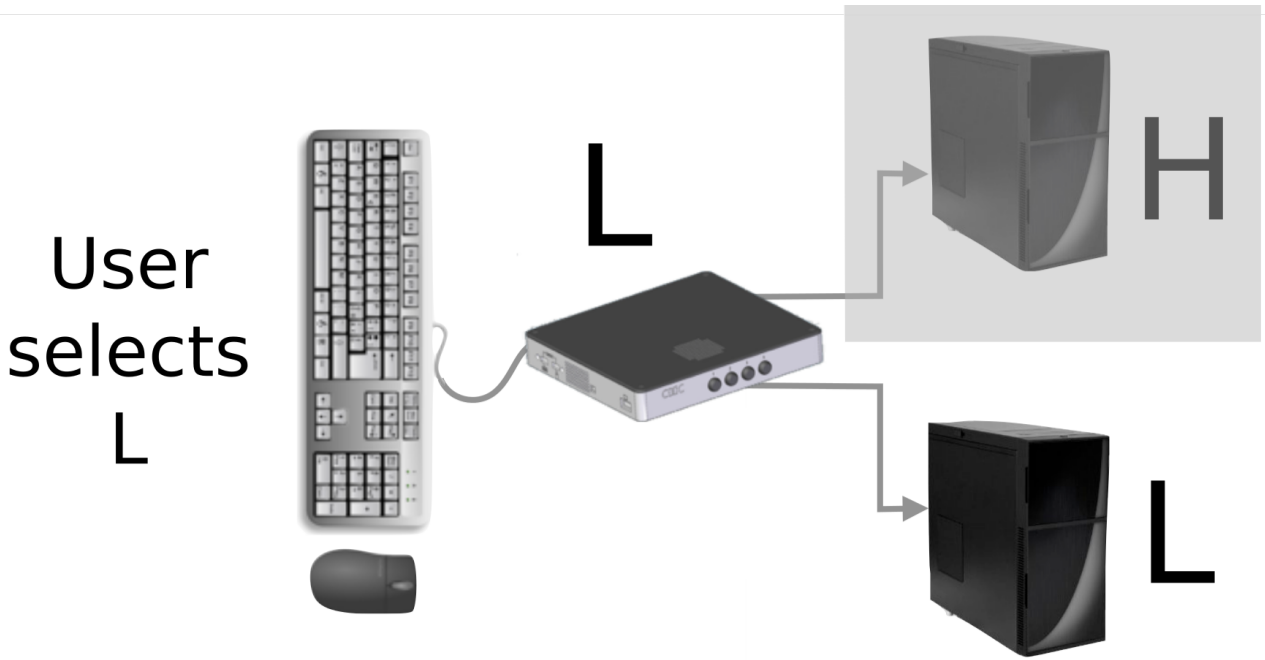

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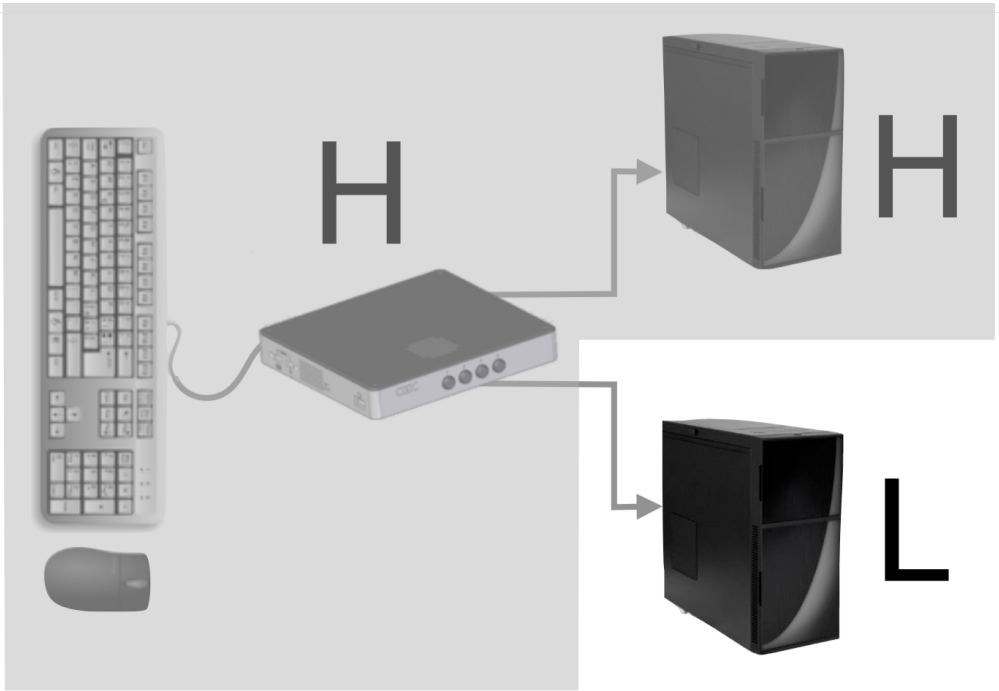

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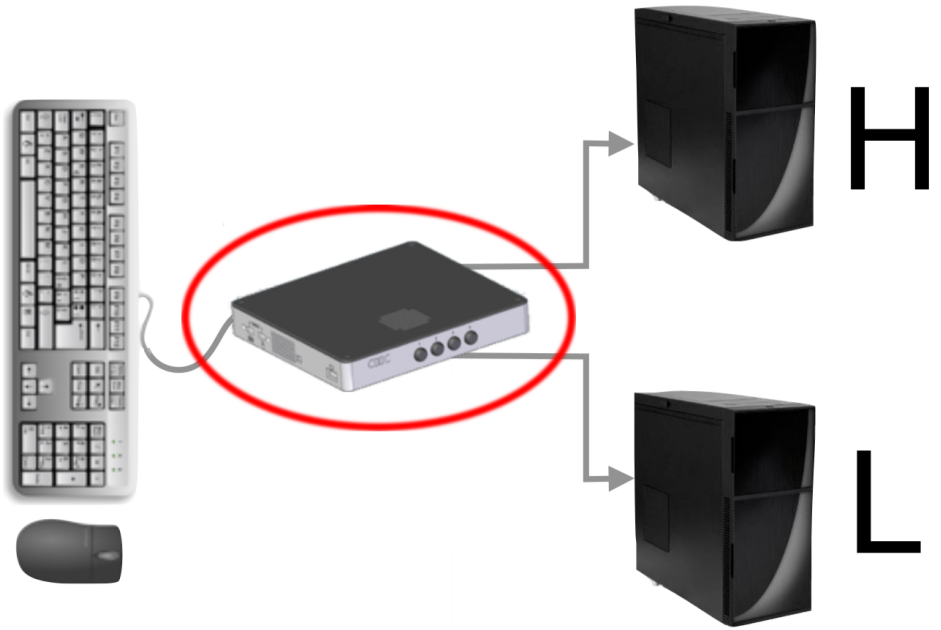

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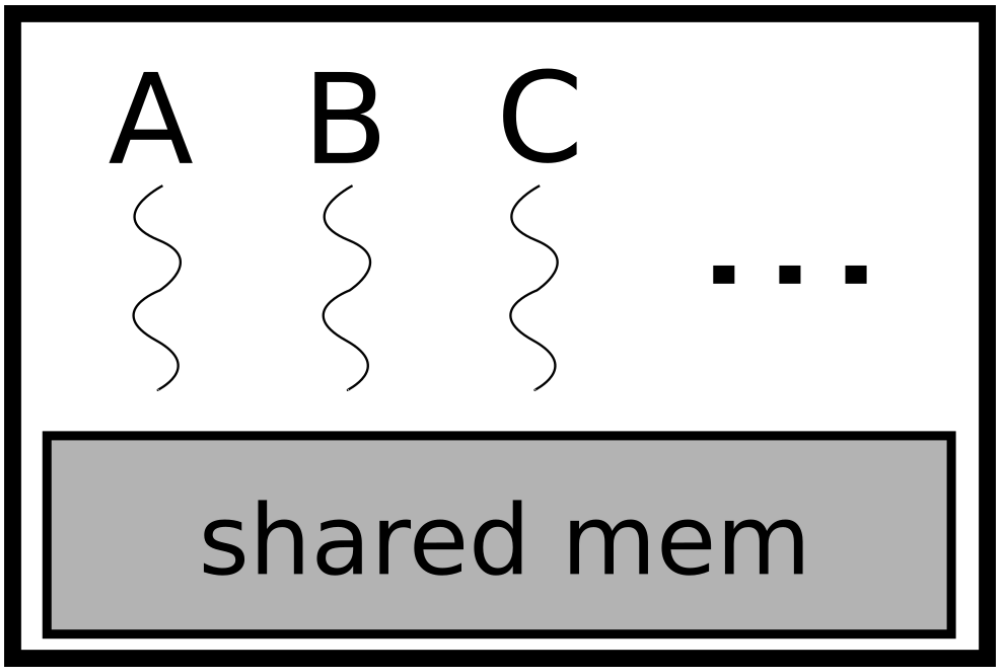

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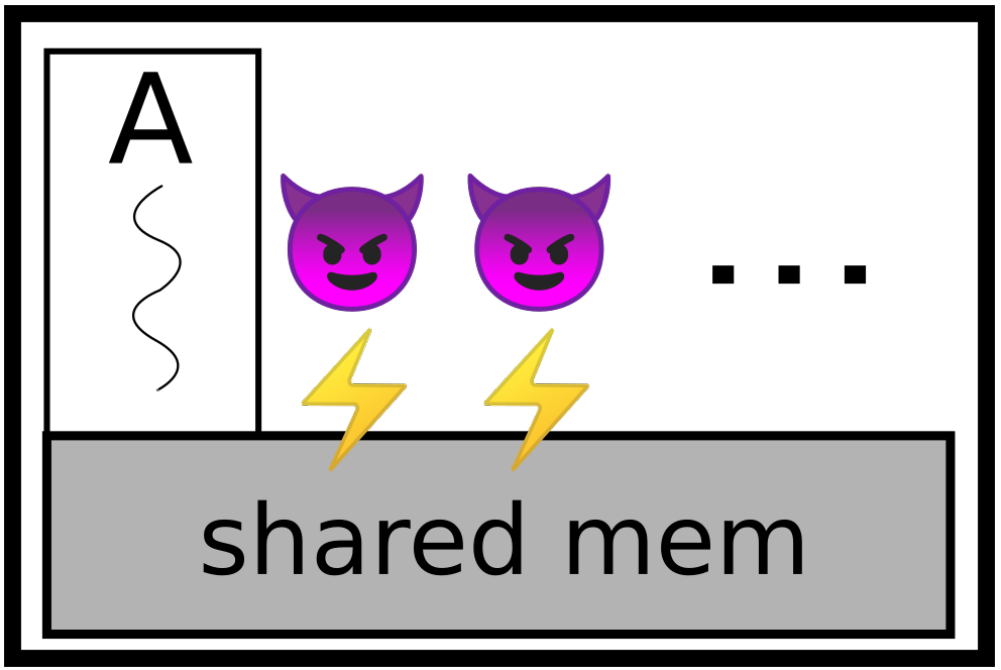

Per-thread, subject to havoc.

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Low, unlocked part of state must remain indistinguishable.

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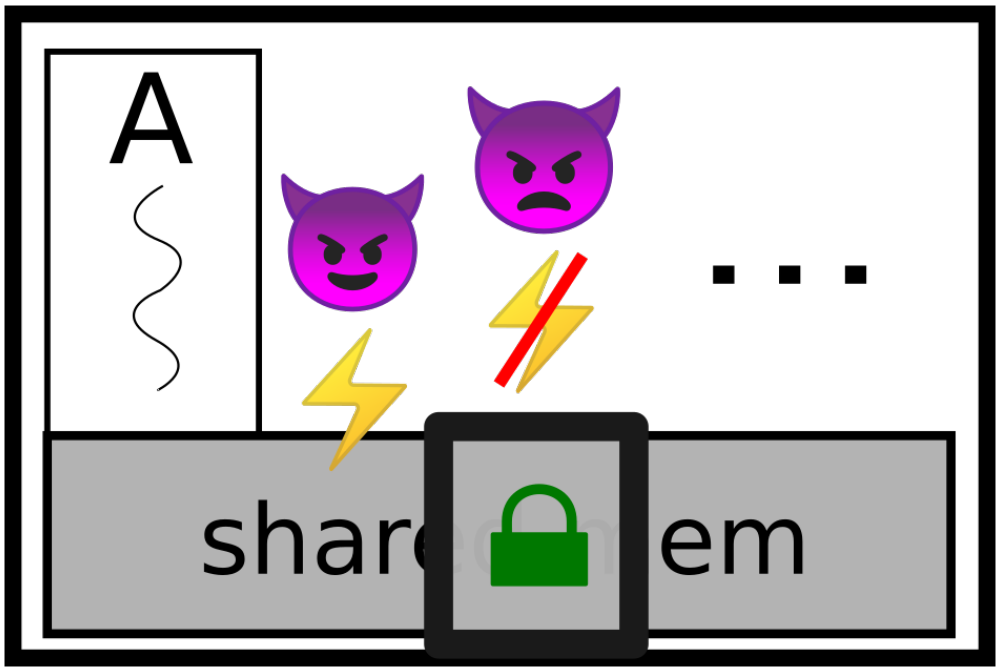

Per-thread, subject to havoc that obeys locking discipline.

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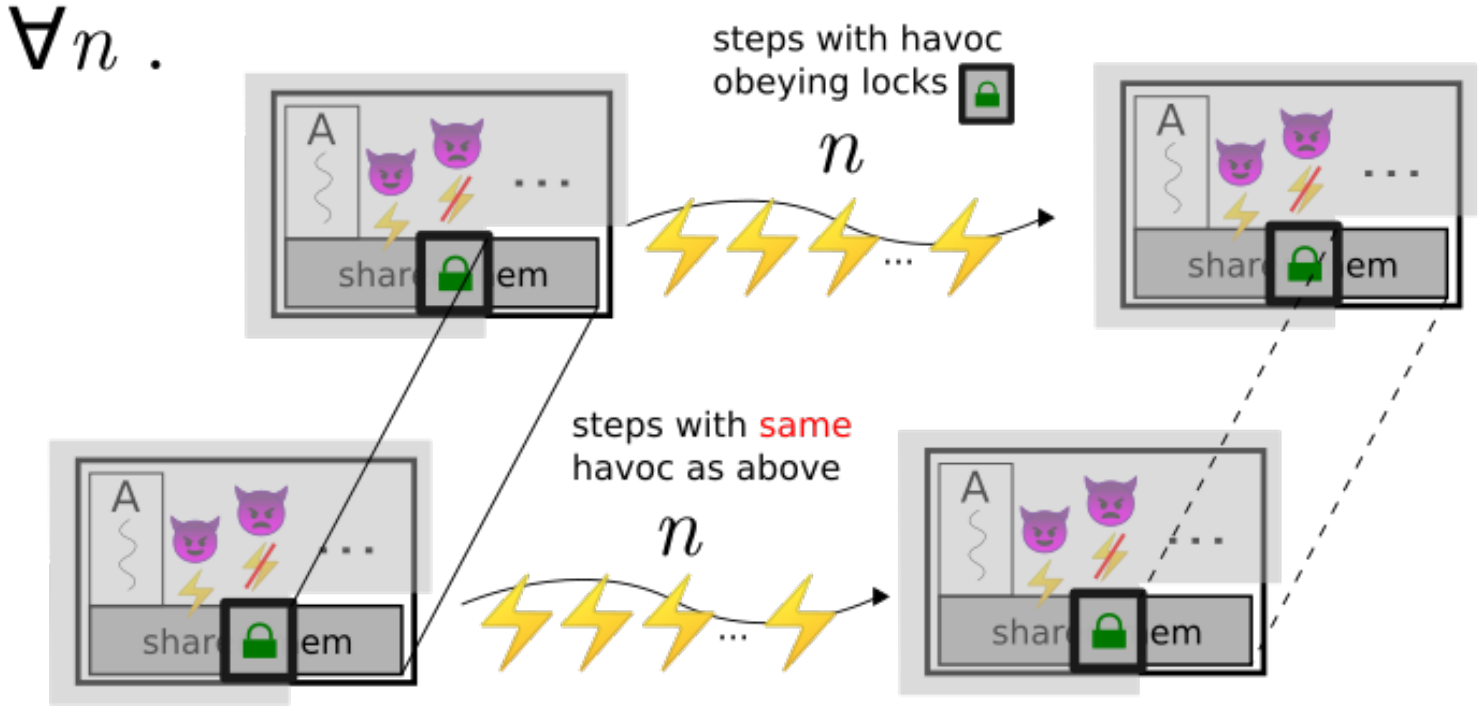
Per-thread compositional property:



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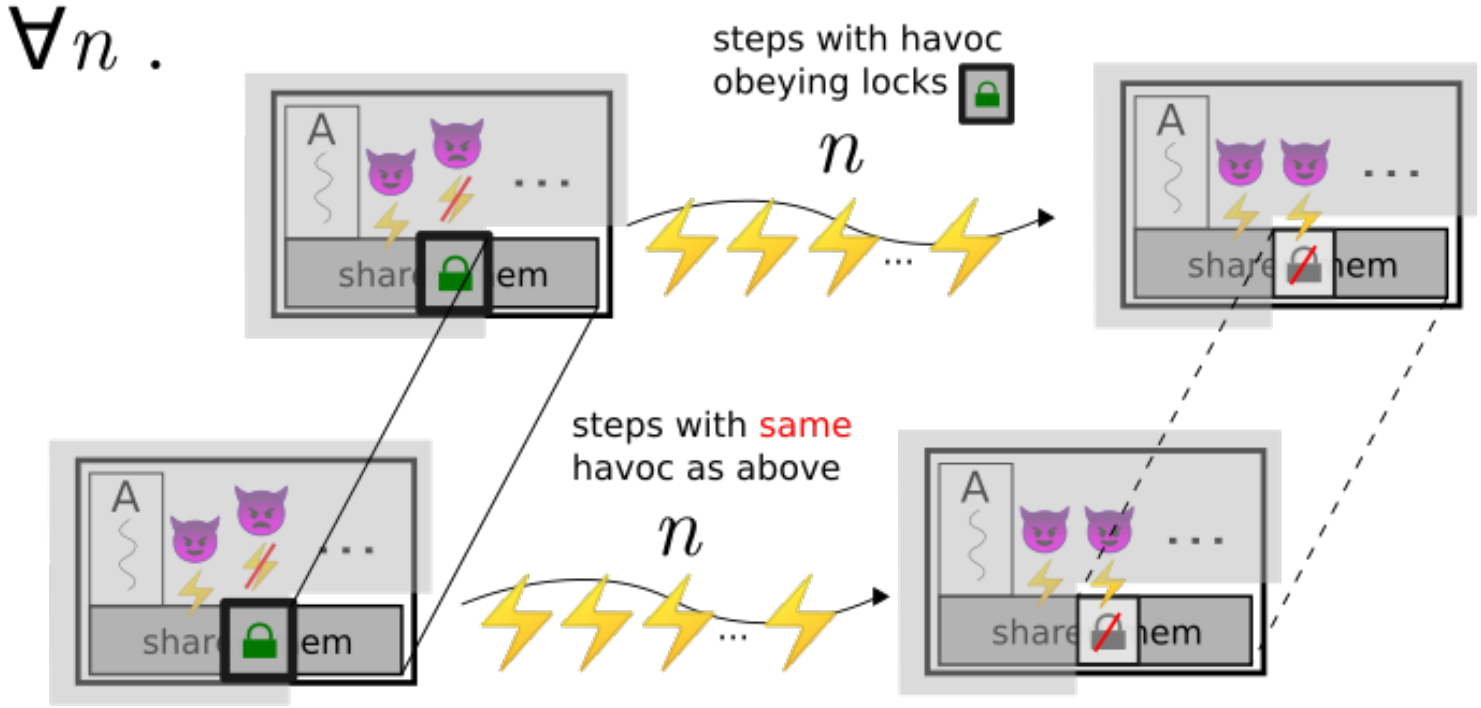

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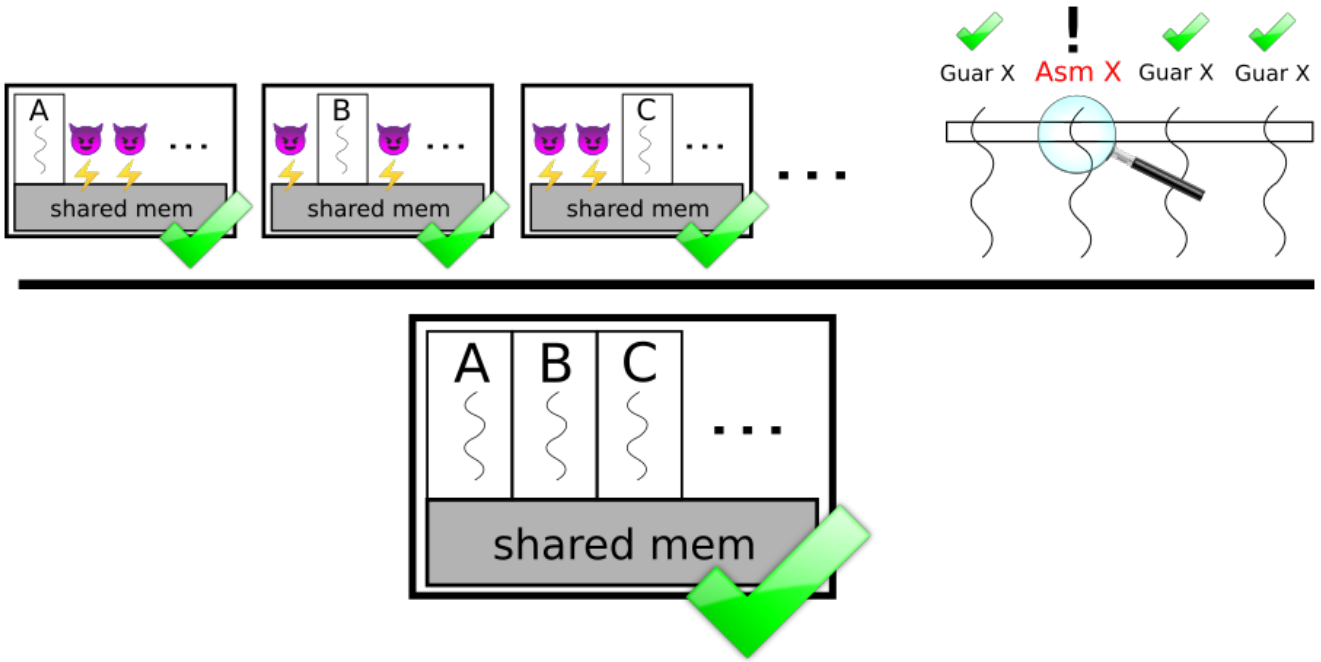
Per-thread compositionality theorem [Murray+, CSF'16]:



Under the hood: *assume-guarantee* on variable access.

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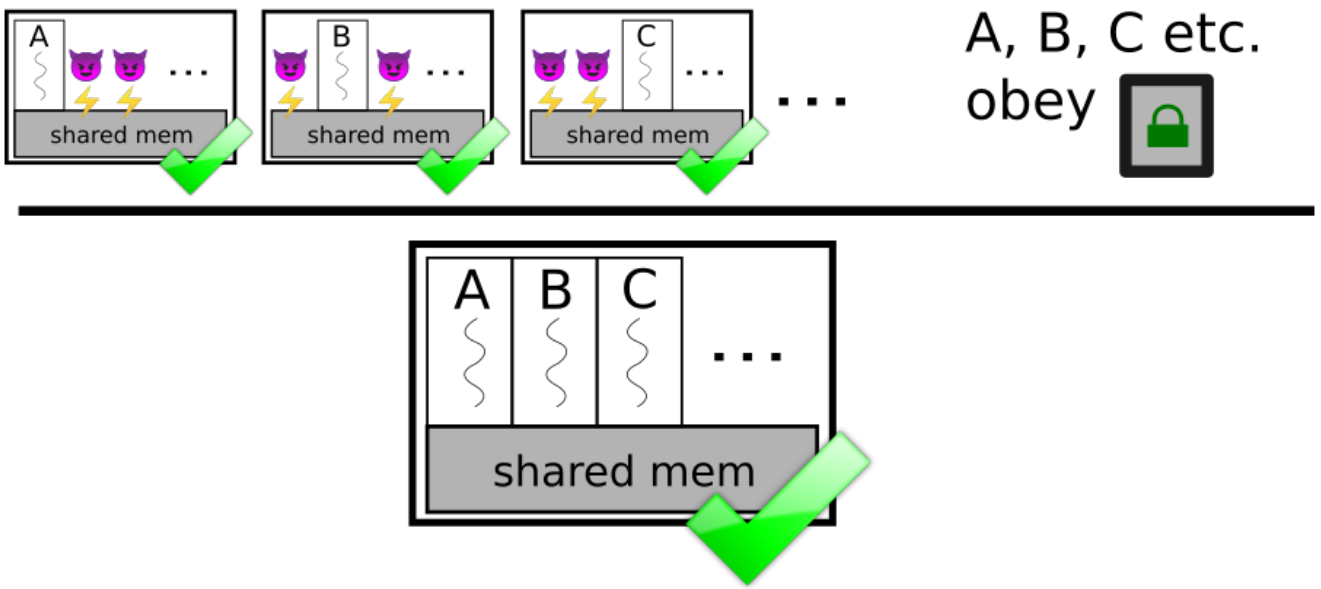
Per-thread compositionality theorem:



[Murray+, CSF'16] instantiated with locking primitives.

The confidentiality property

Concurrent value-dependent noninterference.

Simplest policy: **H**igh $\not\to$ **L**ow

Low, unlocked part of state must remain indistinguishable.

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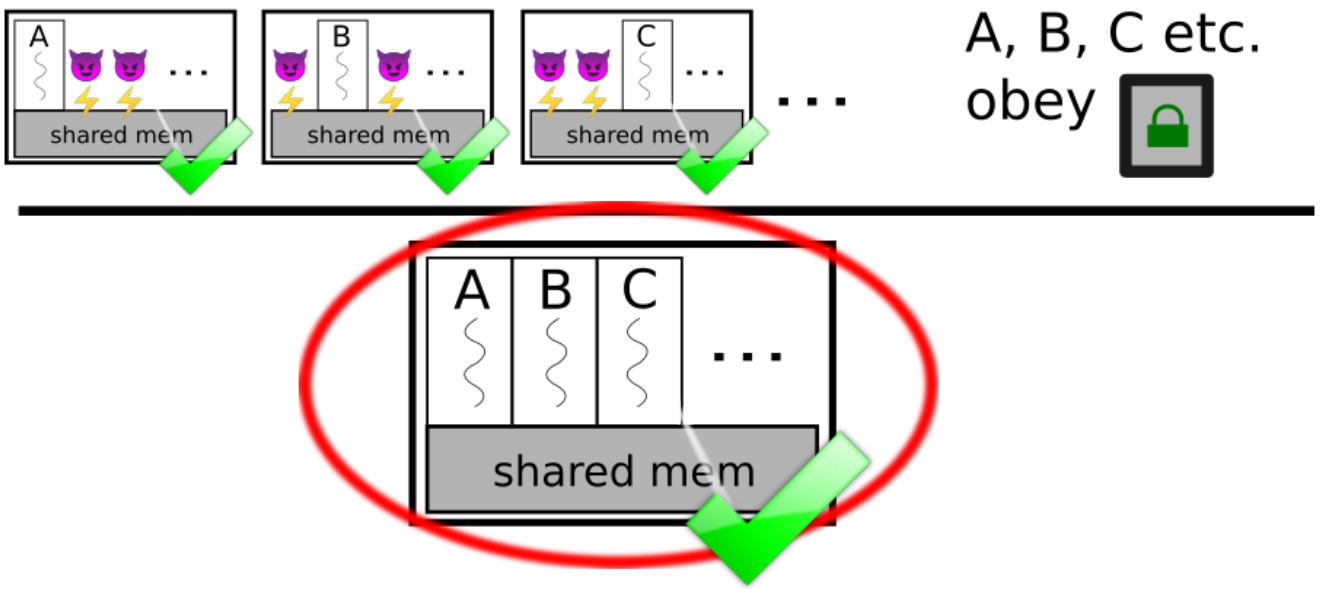
Whole-system property:



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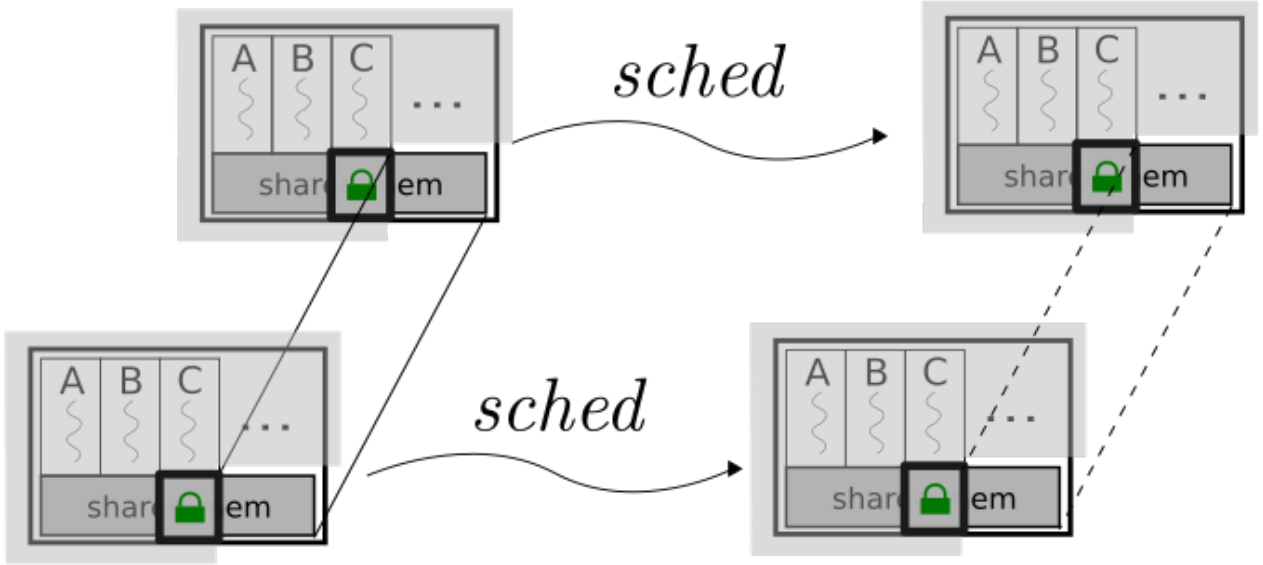

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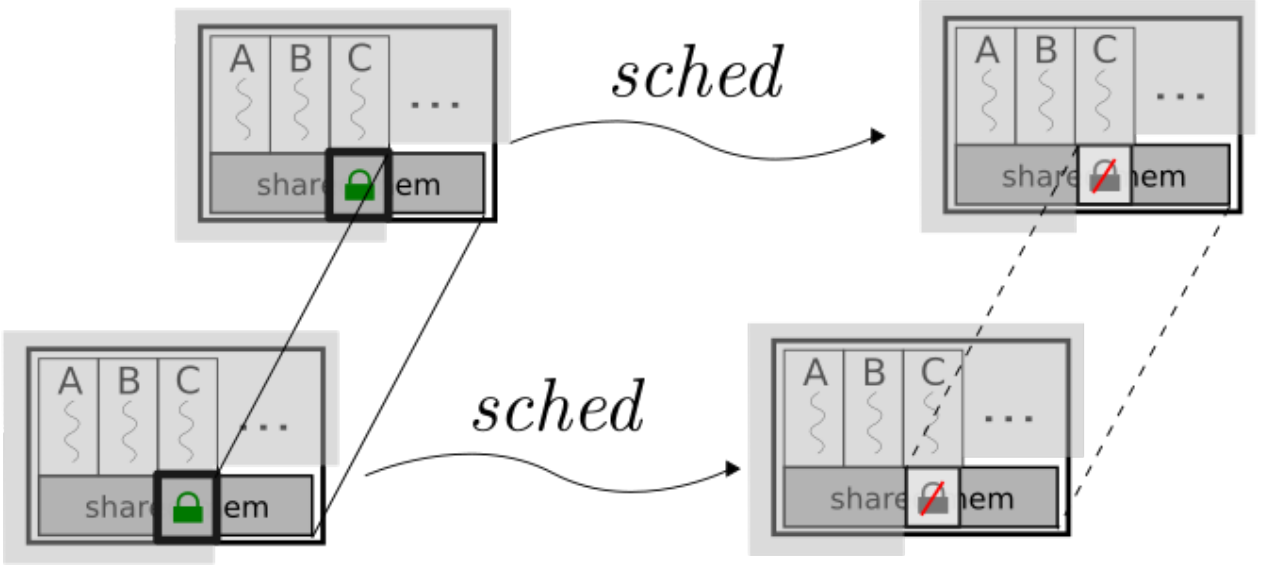

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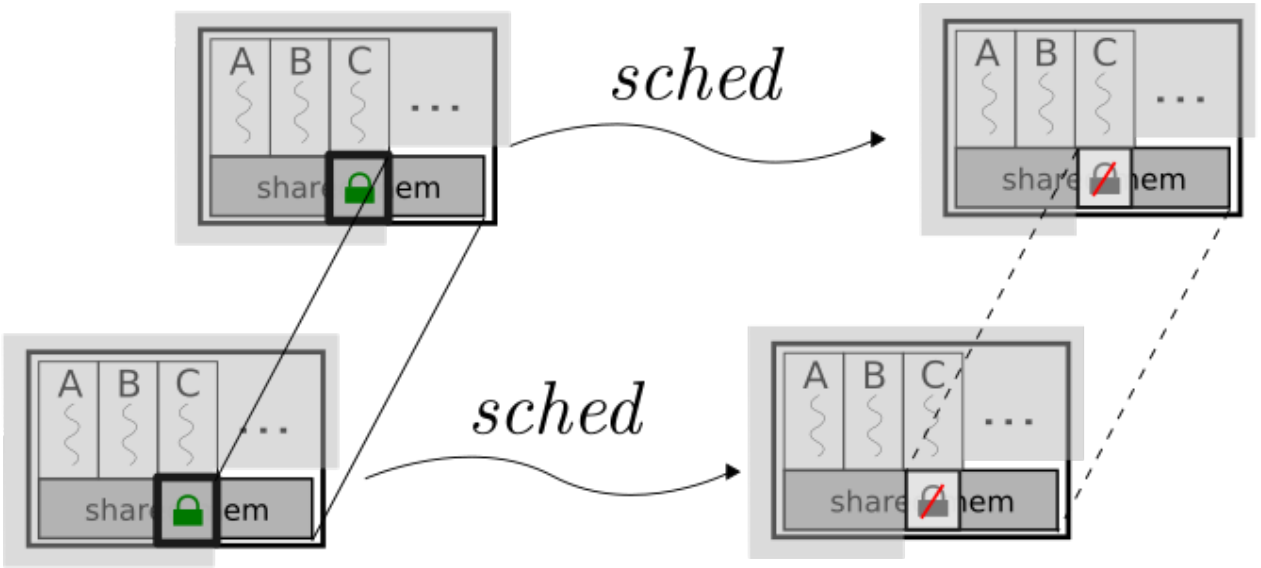


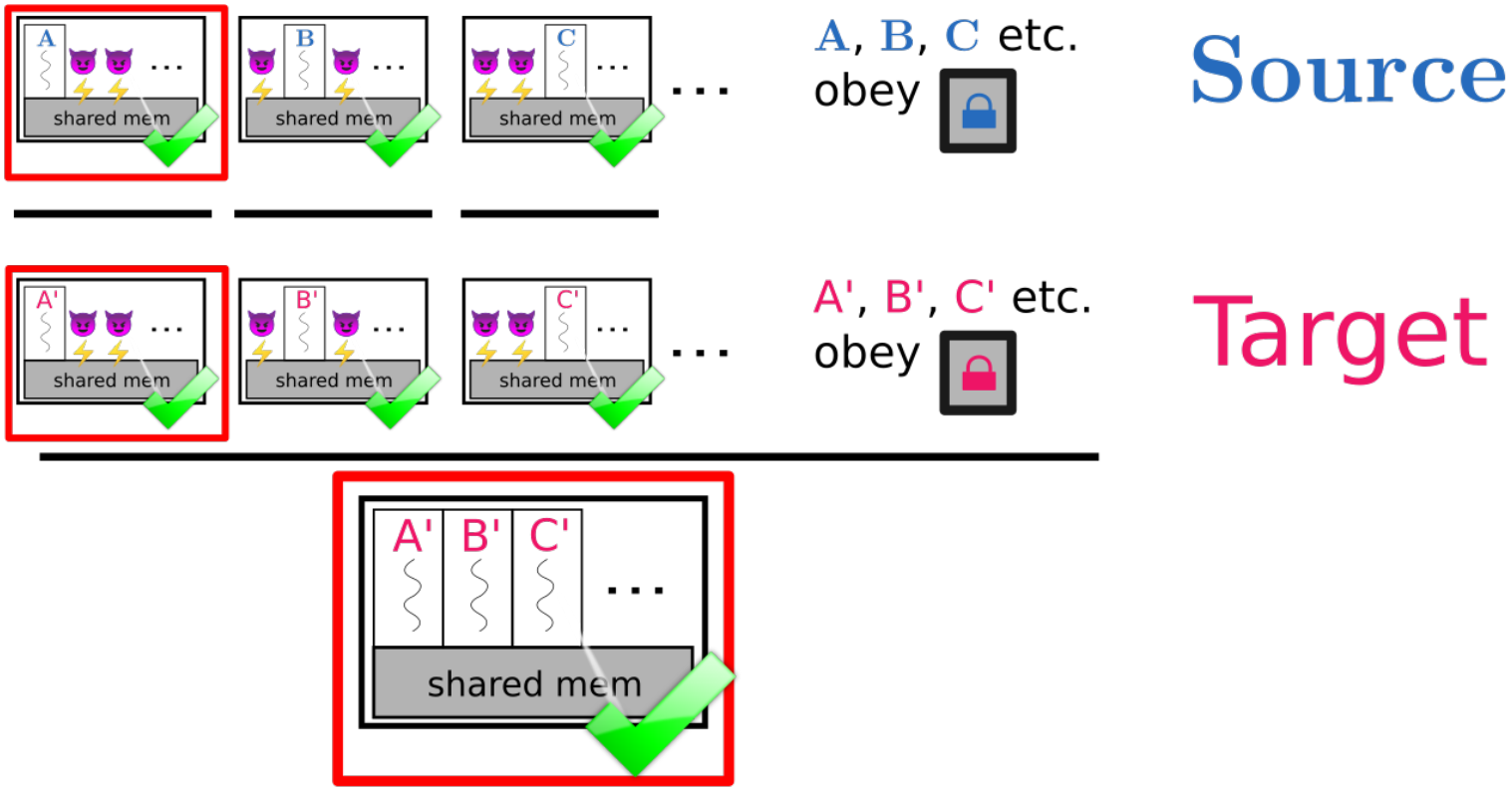
i.e. Locked state still not considered to be observable.

This talk

Part 1: Concurrent value-dependent noninterference

Part 2: Per-thread compositional refinement

Part 3: While-to-RISC compiler verification



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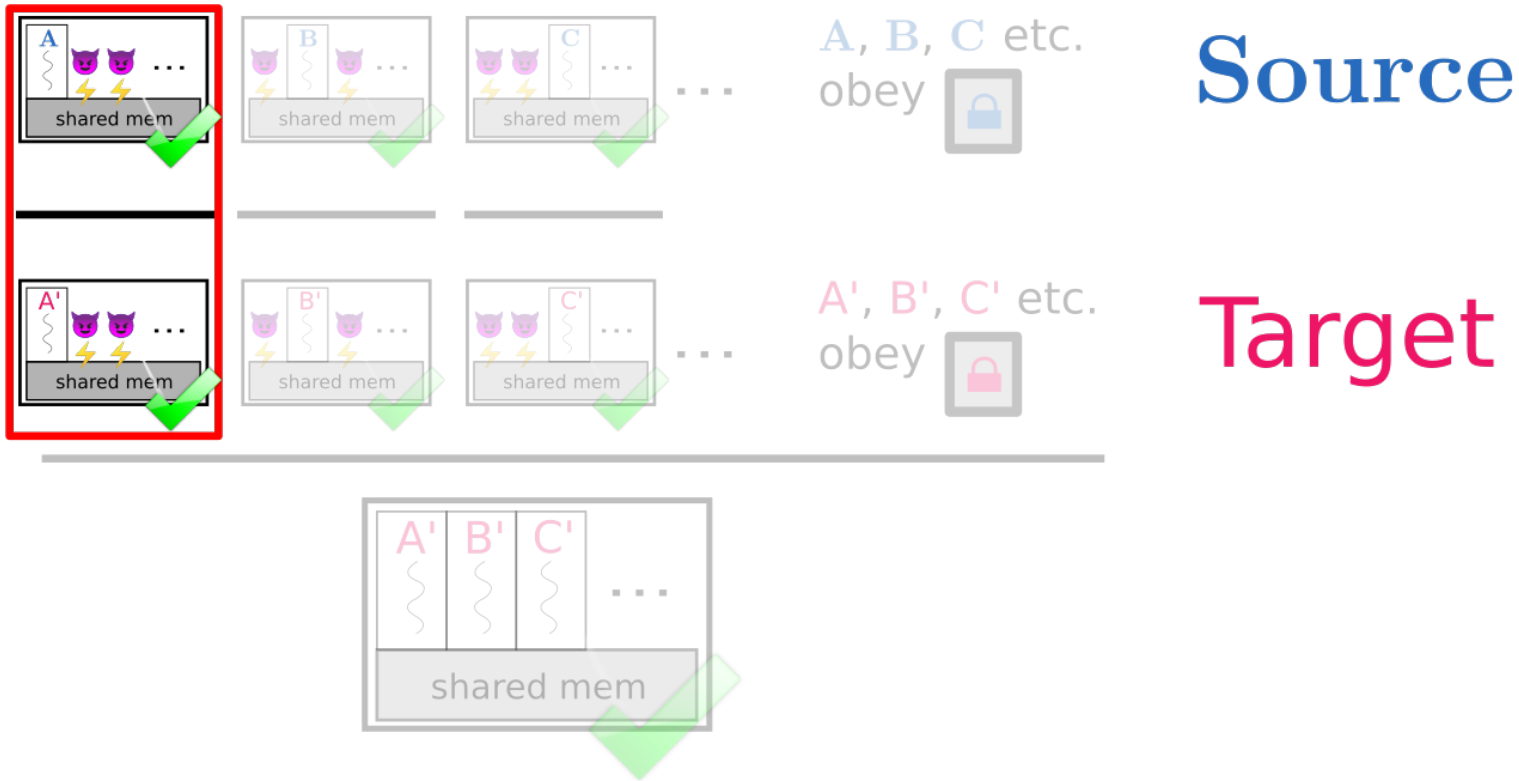
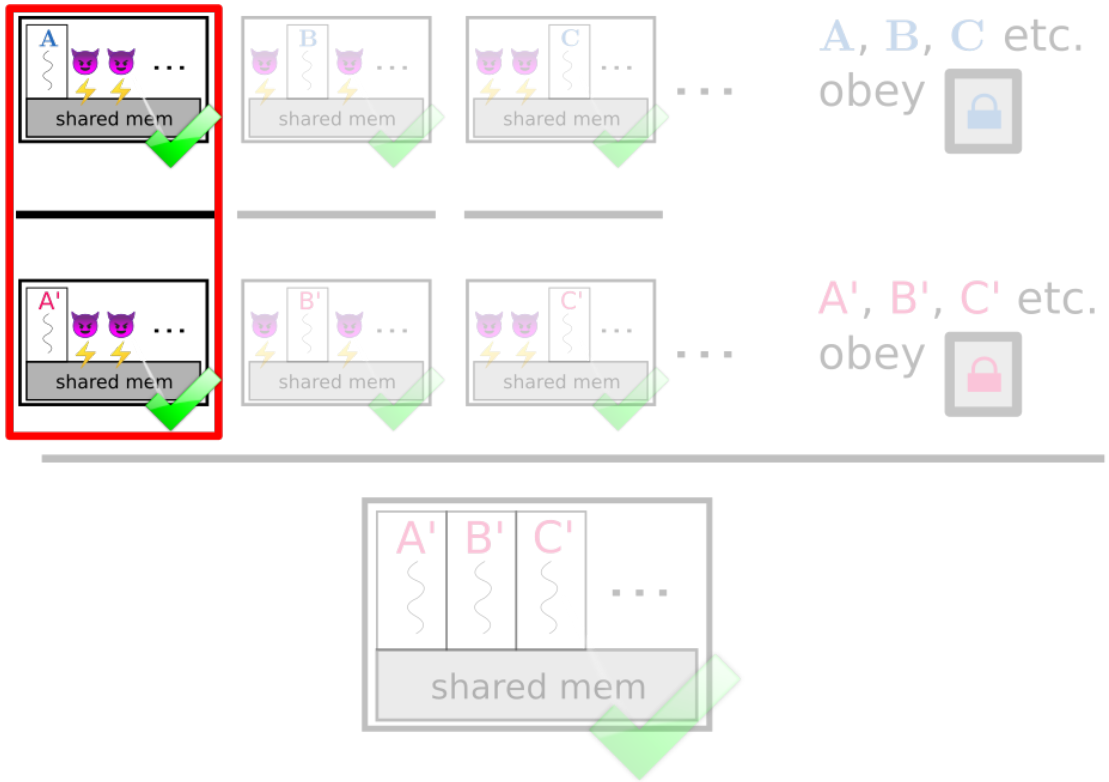


Proof technique for compilation

Per-thread *compositional refinement* [Murray+, CSF'16]



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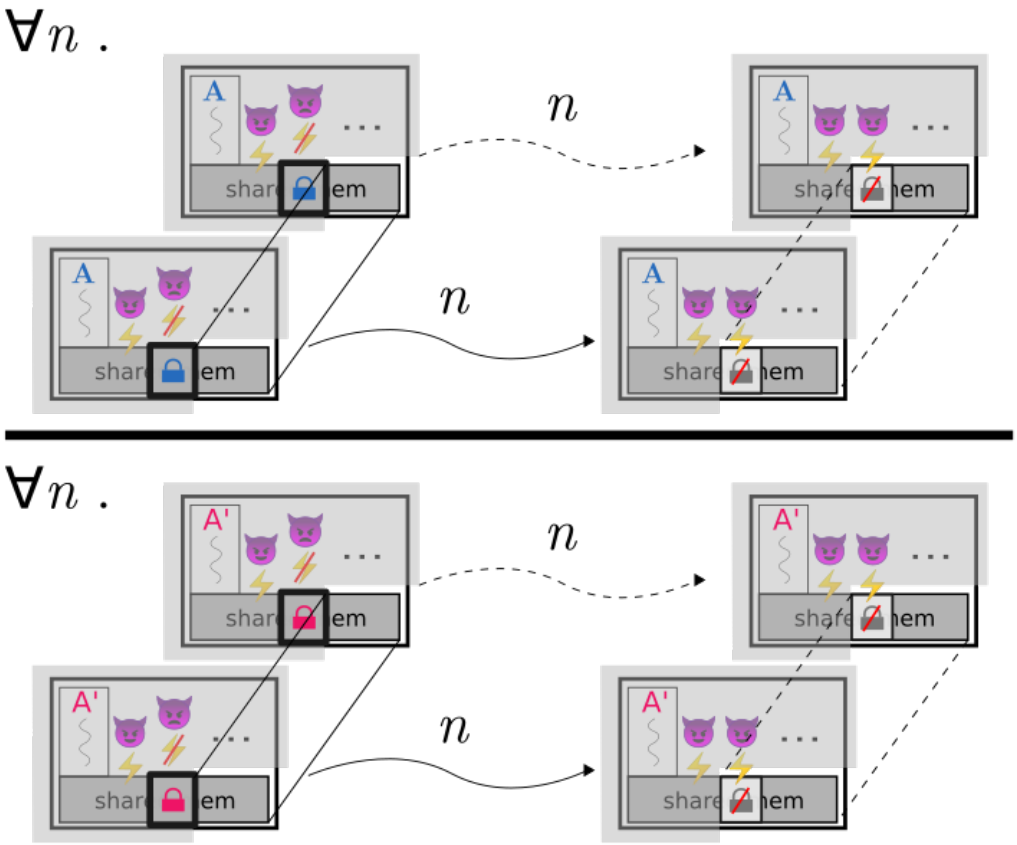

Source

Target

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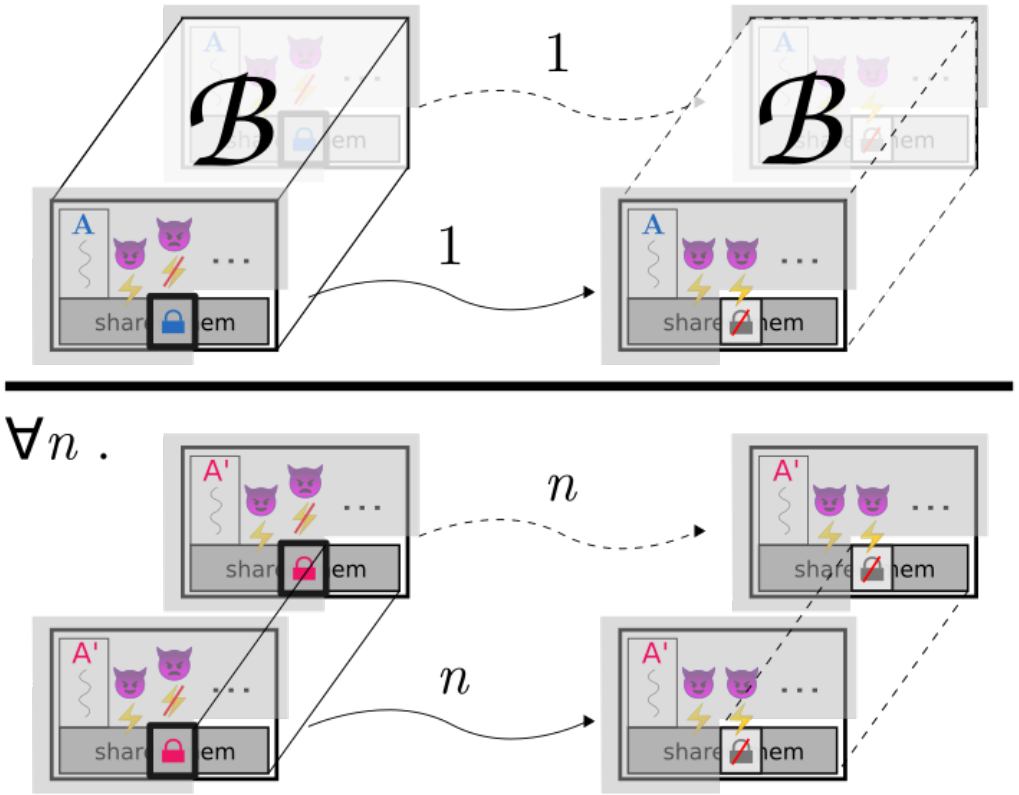
Per-thread *compositional refinement* [Murray+, CSF'16]
Given bisimulation $\mathcal{B}$ establishing the property,



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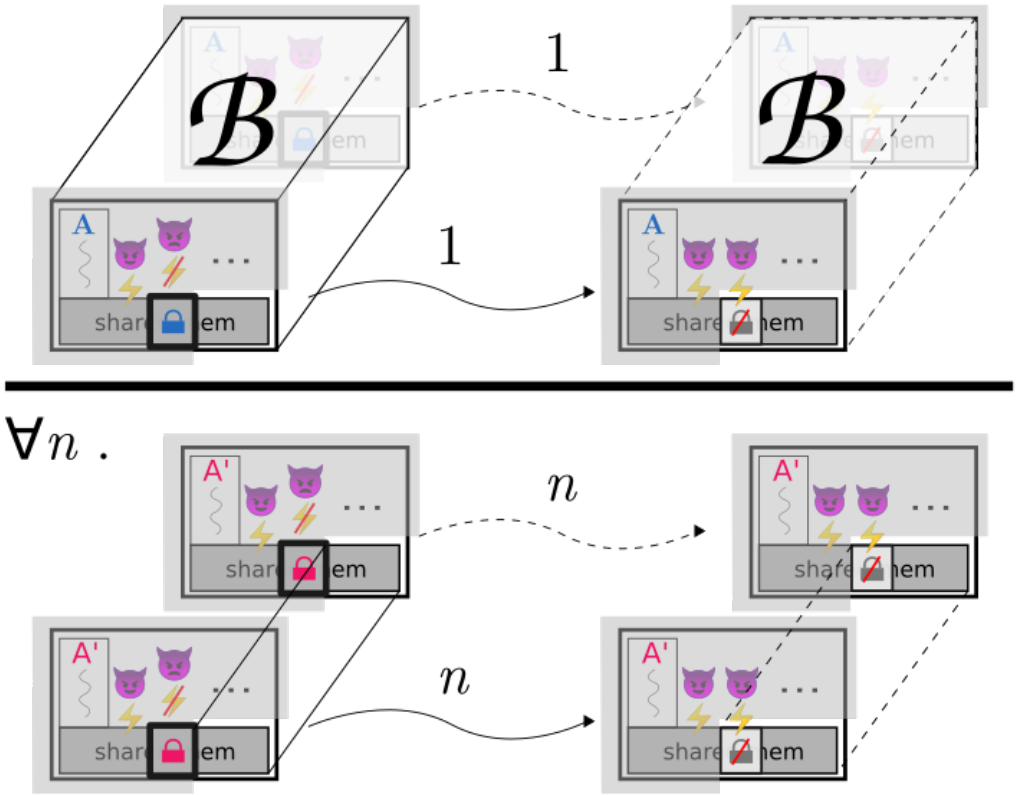

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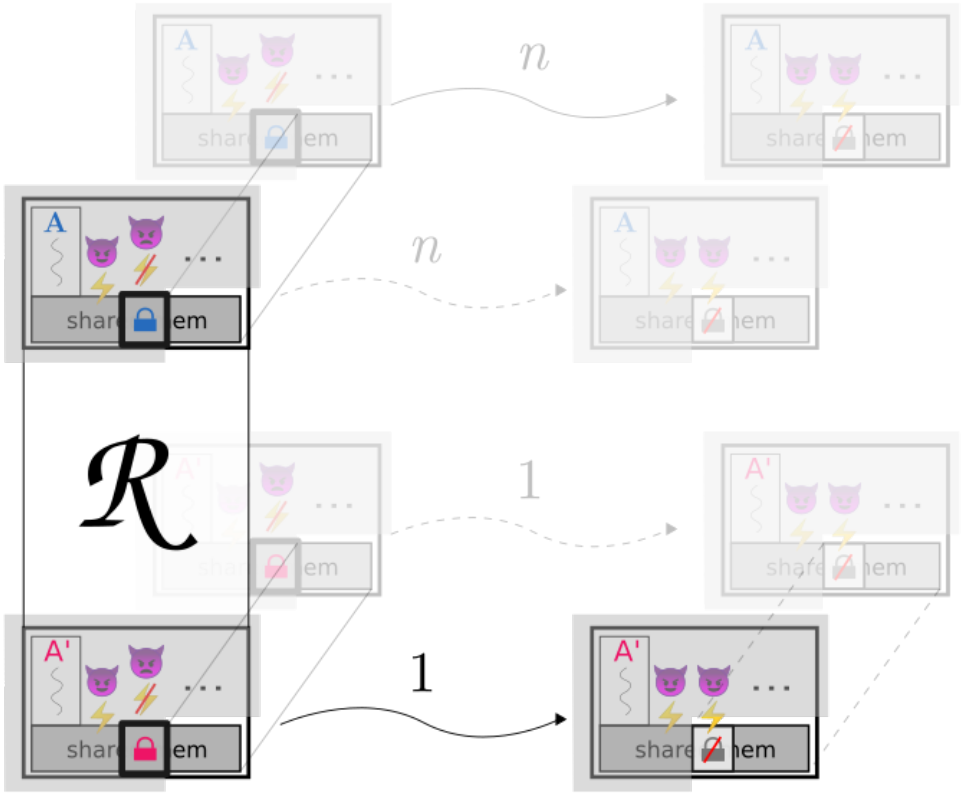
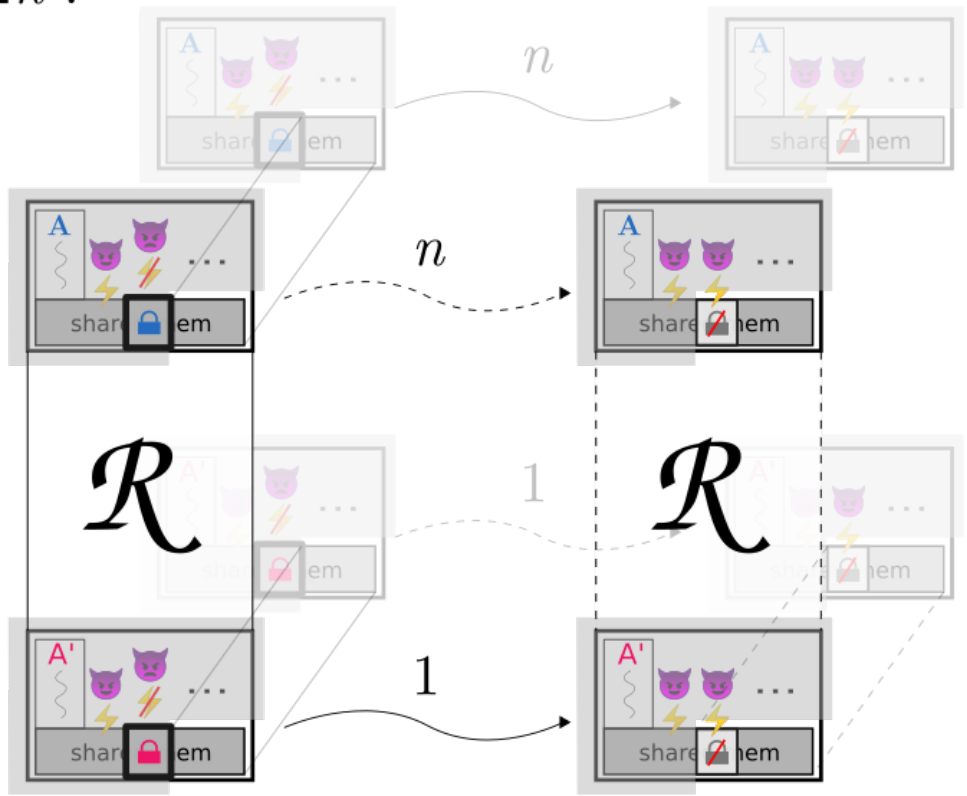


Proof technique for compilation

Per-thread *compositional refinement* [Murray+, CSF'16]

Given bisimulation $\mathcal{B}$ establishing the property, nominate $\mathcal{R}$, $\mathcal{I}$ s.t.:

$\exists n$.



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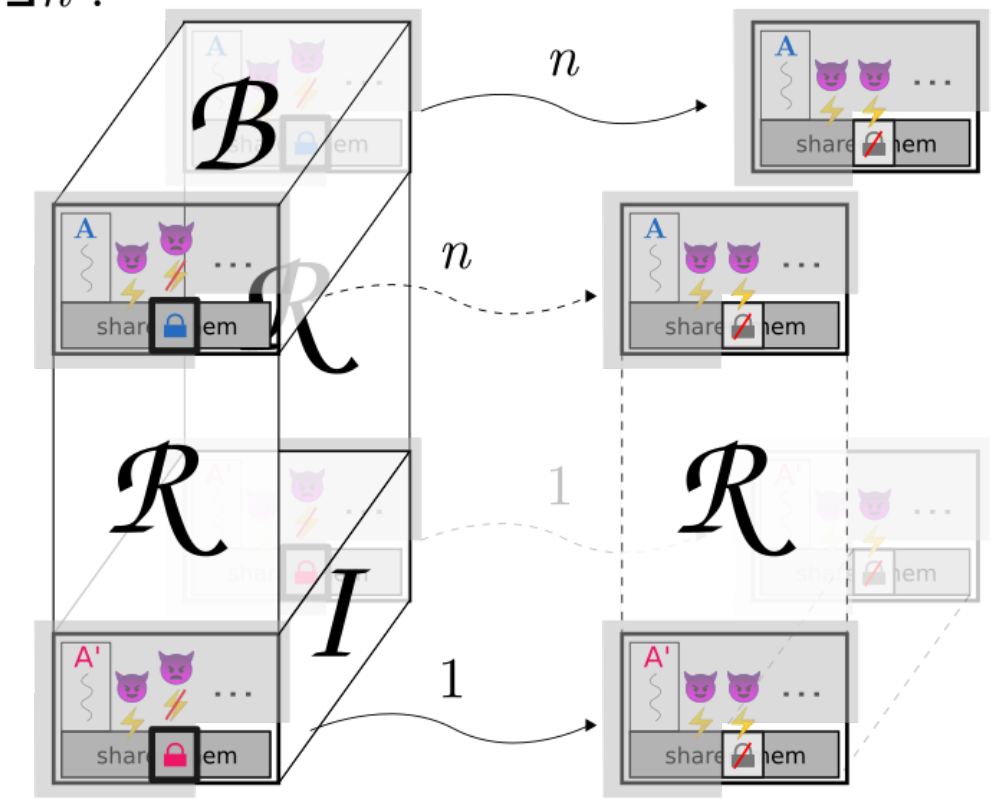

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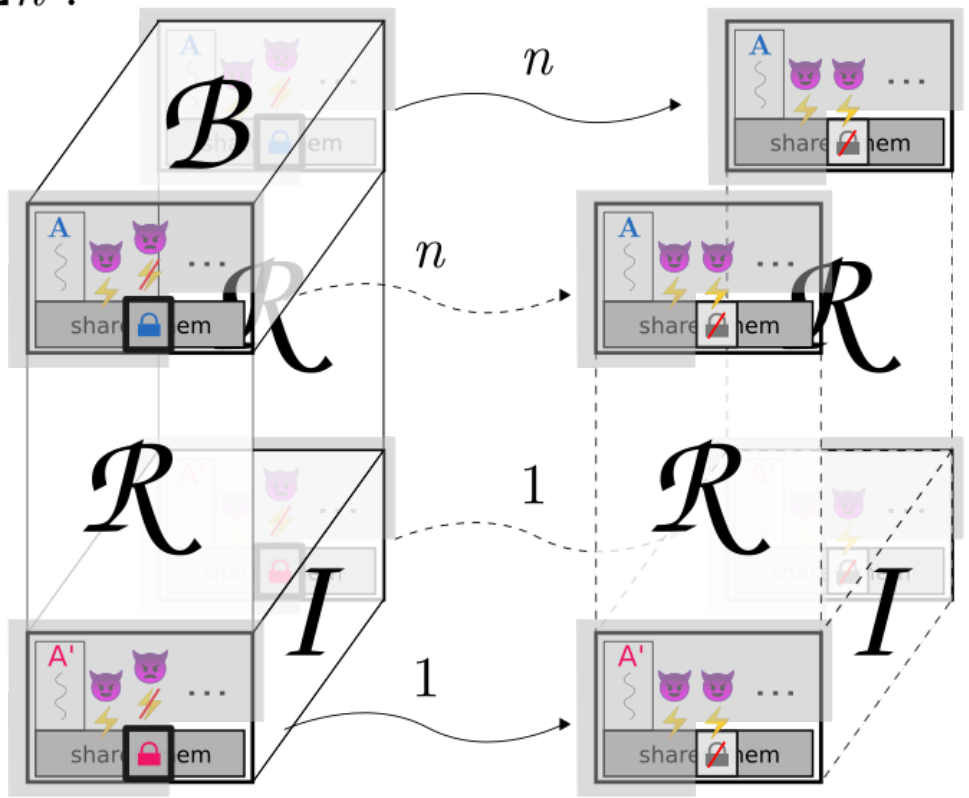
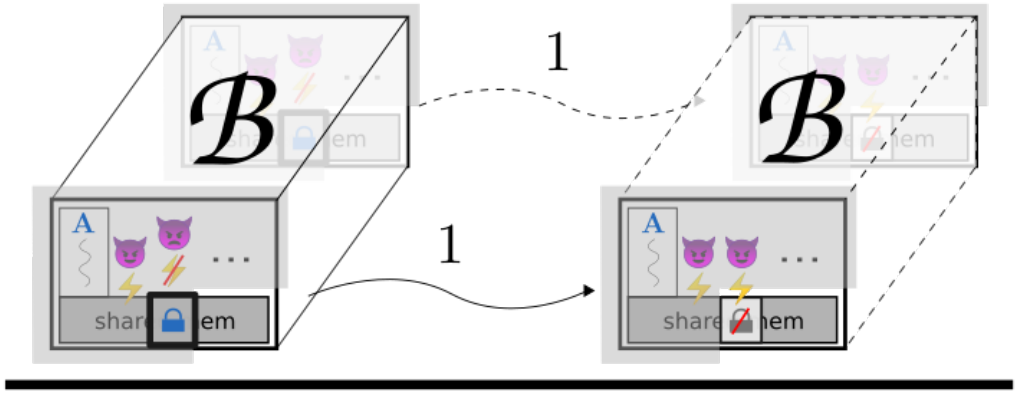


Proof technique for compilation

Per-thread *compositional refinement* [Murray+, CSF'16]
Then $\mathcal{B}'$ $(= \mathcal{B}_T\_of\ \mathcal{B}\ \mathcal{R}\ \mathcal{I})$ establishes the target-level property:



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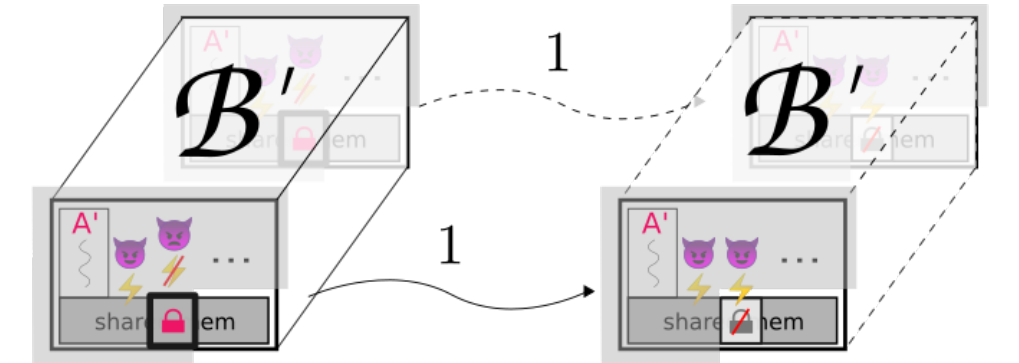
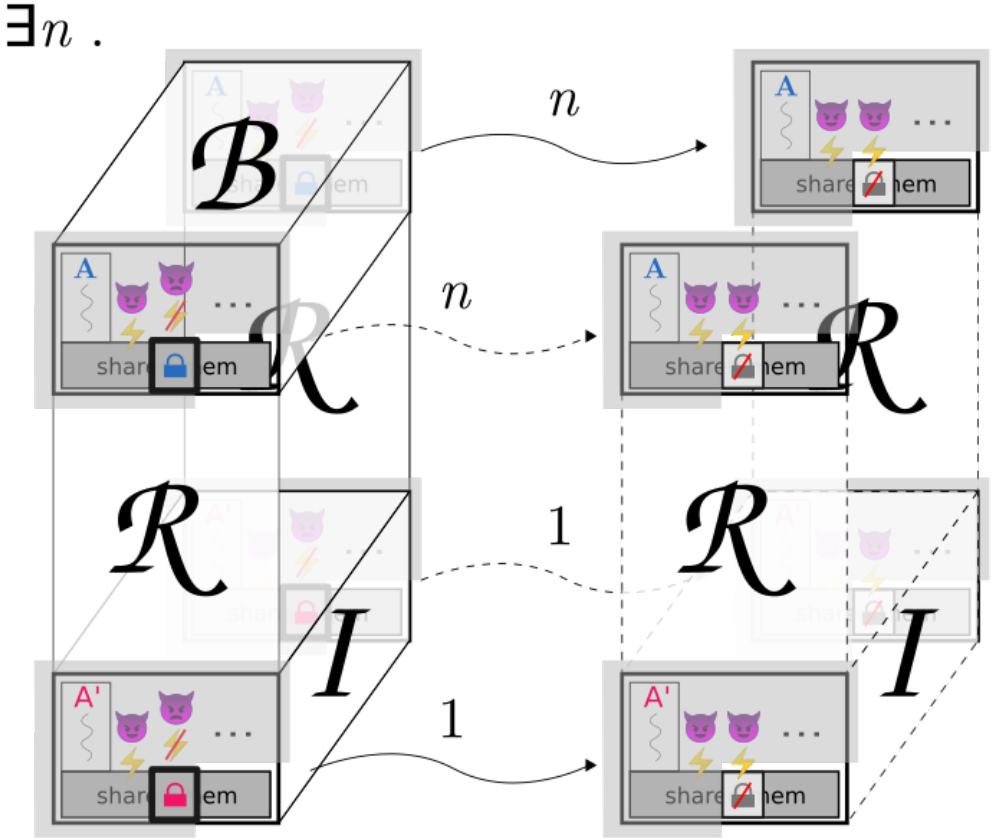


Target

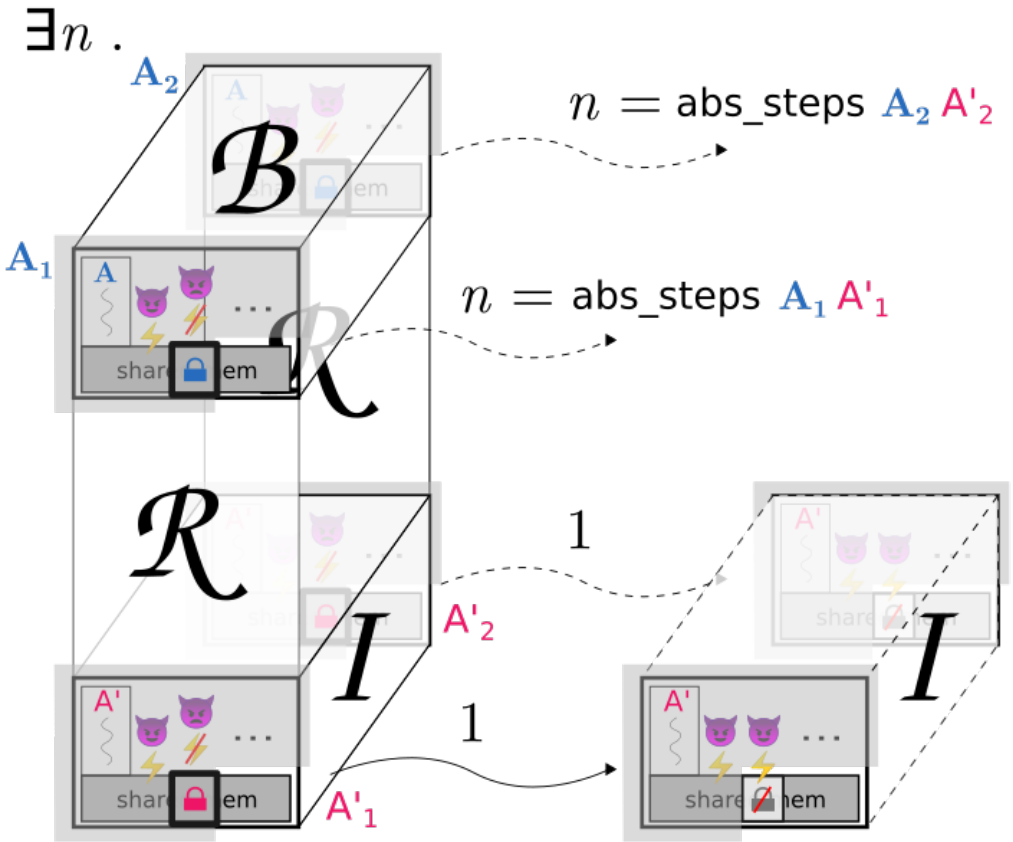
Proof technique for compilation

Simpler proof technique than this!



Proof technique for compilation

Simpler proof technique! Nominate $\mathcal{R}$, $\mathcal{I}$, abs_steps s.t.



(See: `https://www.isa-afp.org/entries/Dependent_SIFUM_Refinement.html`)

Proof technique for compilation

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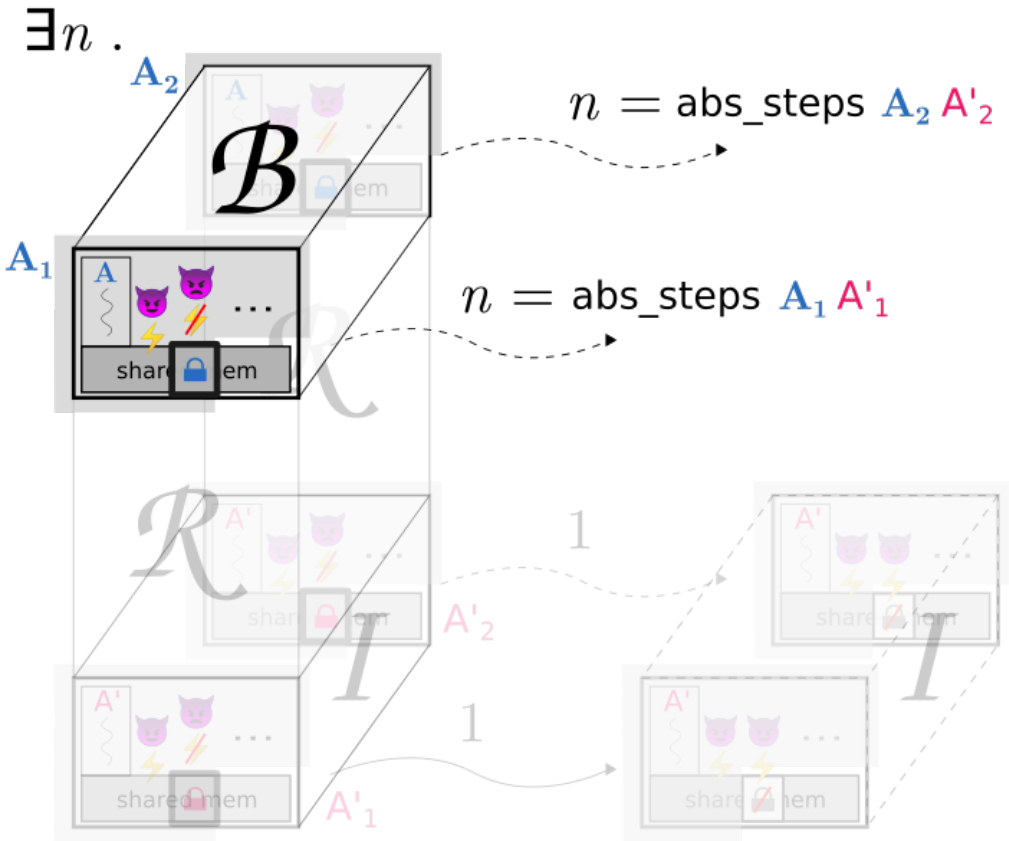

Easy to prove if no H-branching in $\mathbf{A}$

(See: `https://www.isa-afp.org/entries/Dependent_SIFUM_Refinement.html`)

Proof technique for compilation

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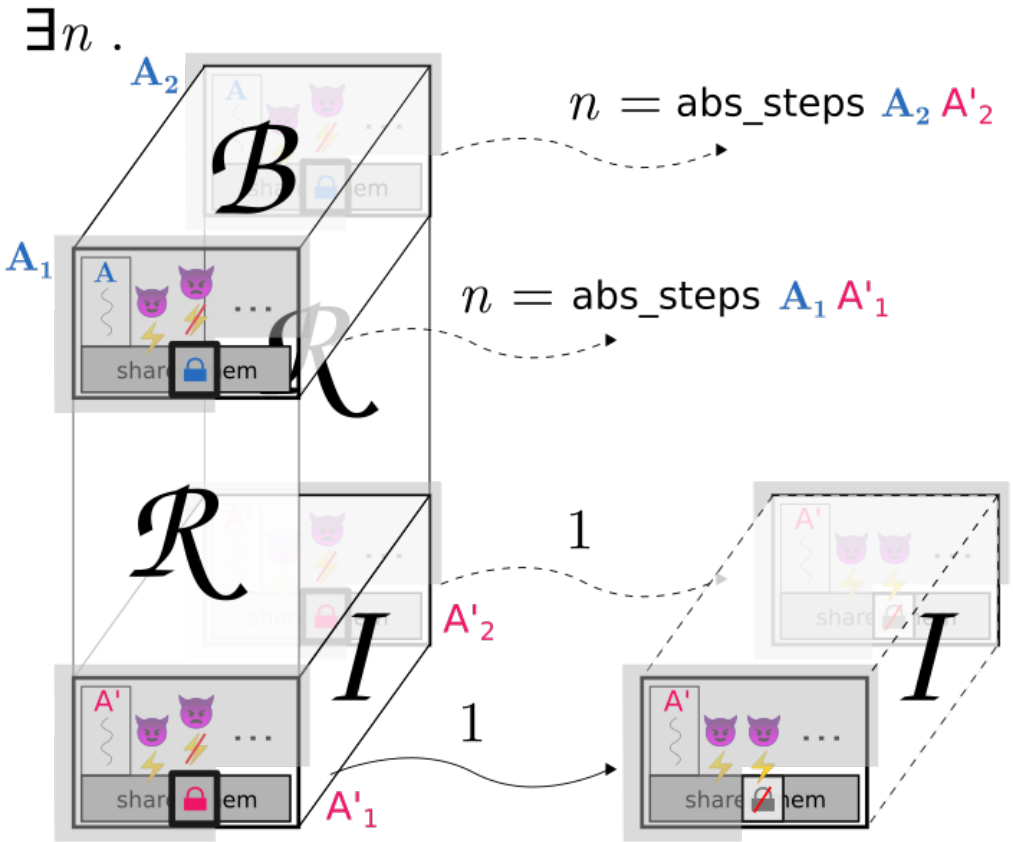


($\mathcal{I}$ as pc-security)

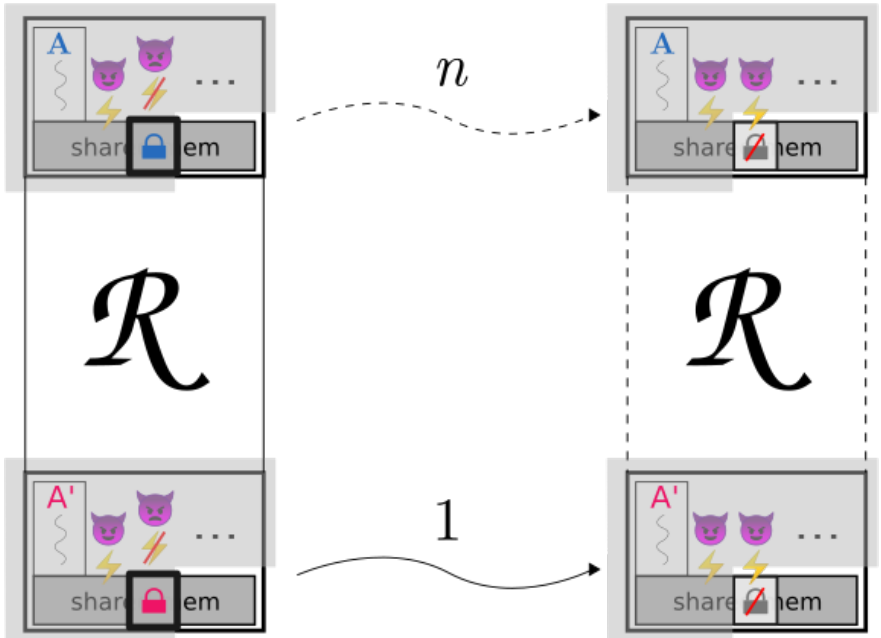
Easy to prove if no H-branching in $\mathbf{A}$, and no new H-branching.

(See: `https://www.isa-afp.org/entries/Dependent_SIFUM_Refinement.html`)

Proof technique for compilation

Simpler proof technique! Nominate $\mathcal{R}$, $\mathcal{I}$, abs_steps.
Then it suffices to prove:

$\exists n \;.\; n =$ abs_steps **A** A'



i.e. $\mathcal{R}$ a *simulation* of A' by **A**.

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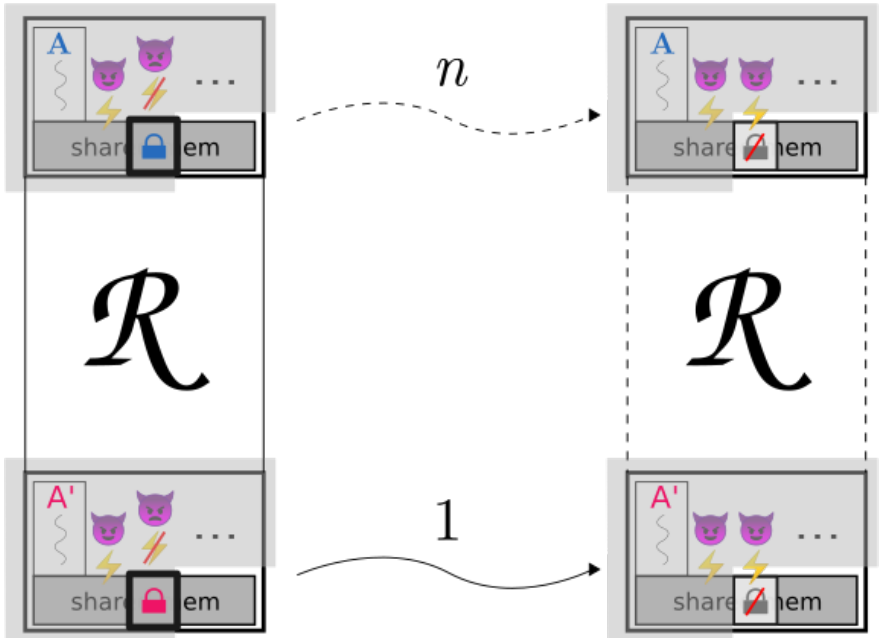
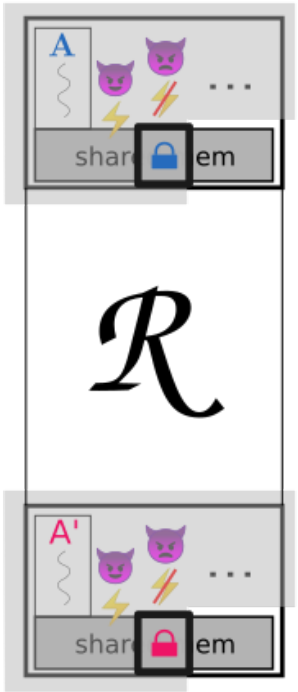


i.e. $\mathcal{R}$ a *simulation* of A' by **A**, with provisos...

Proof technique for compilation

Provisos for $\mathcal{R}$, $\mathcal{I}$:

- $\mathcal{R}$ must preserve shared memory contents and locking state.
  - Under the hood: preserve assumptions and guarantees.



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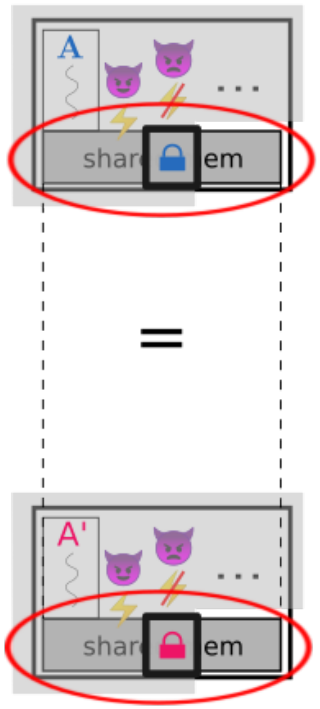

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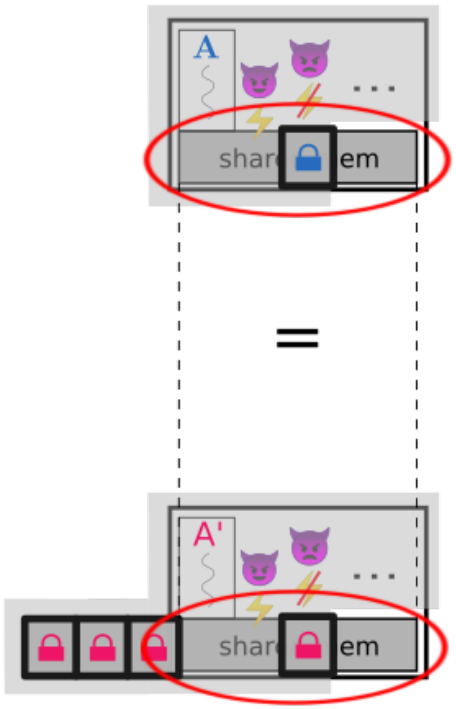

+ any new locations permanently locked.

i.e. No new shared state.

Proof technique for compilation

Provisos for $\mathcal{R}$, $\mathcal{I}$:

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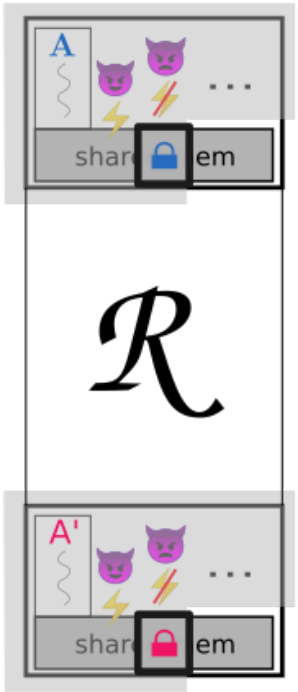

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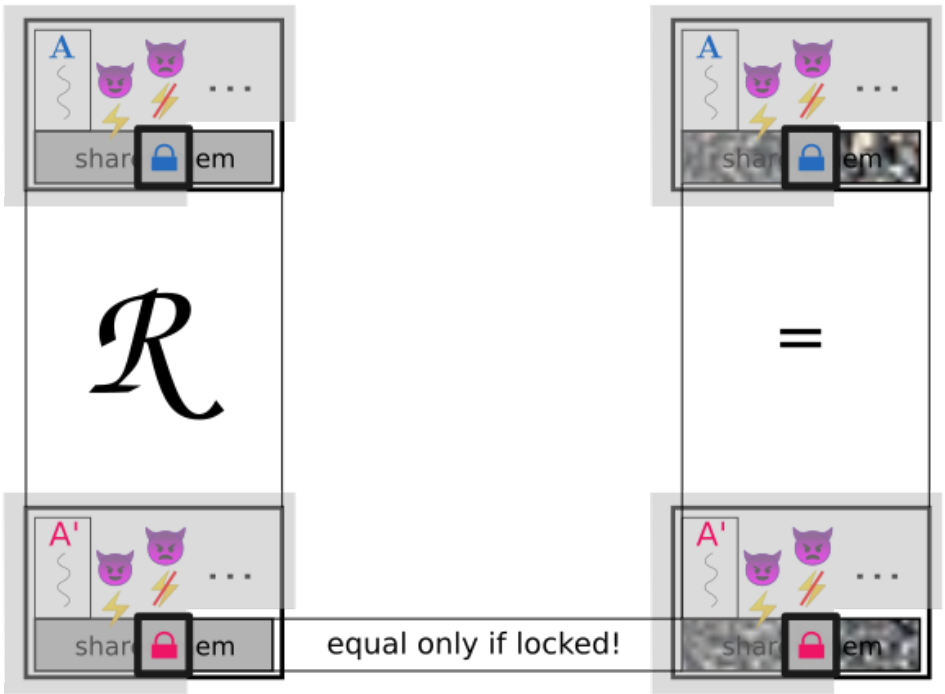

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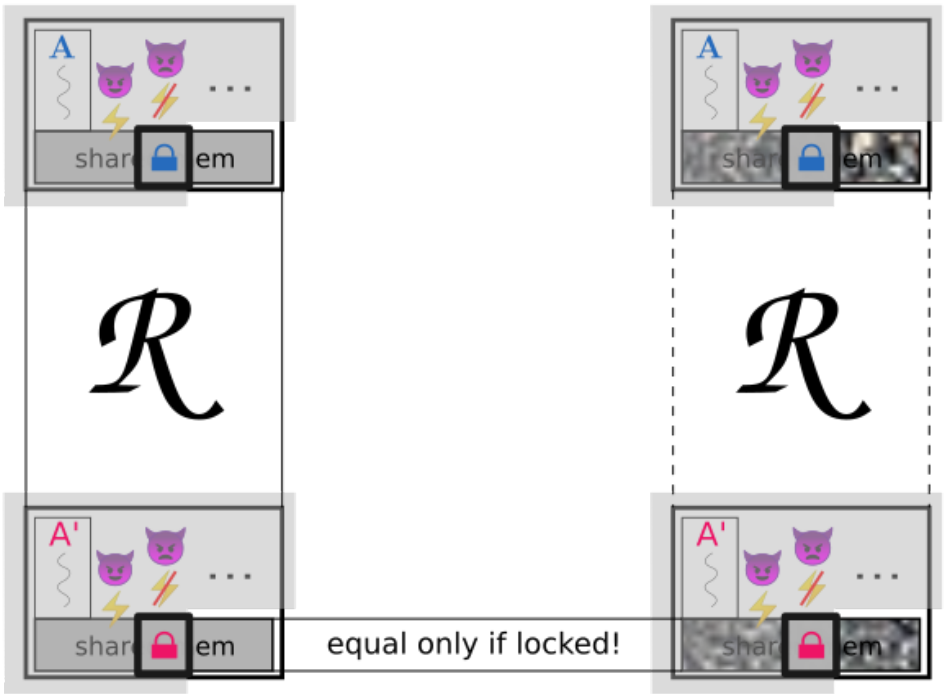

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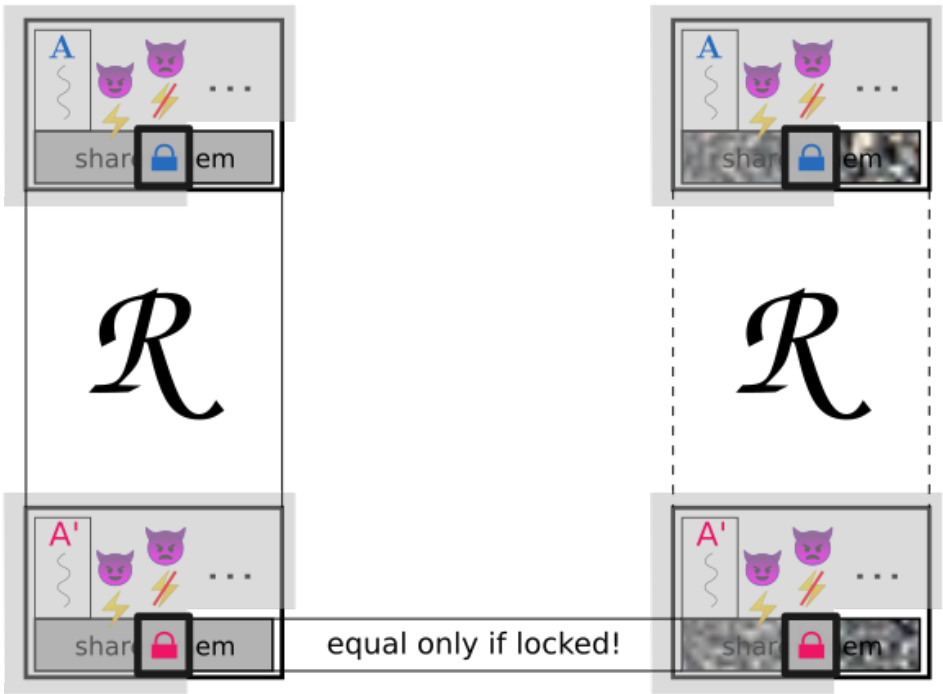


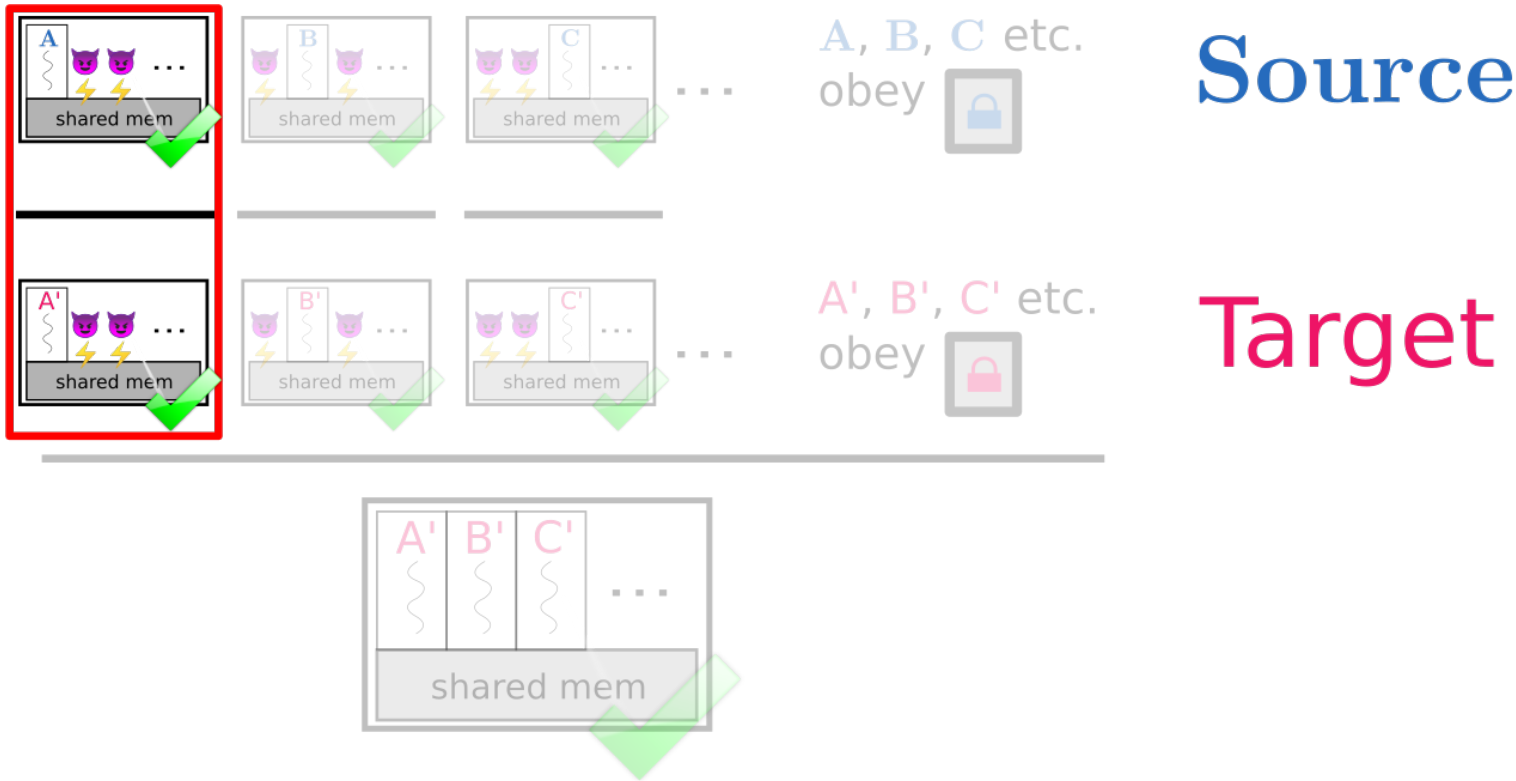
Similar for $\mathcal{I}$.

This talk

Part 1: Concurrent value-dependent noninterference

Part 2: Per-thread compositional refinement

Part 3: While-to-RISC compiler verification



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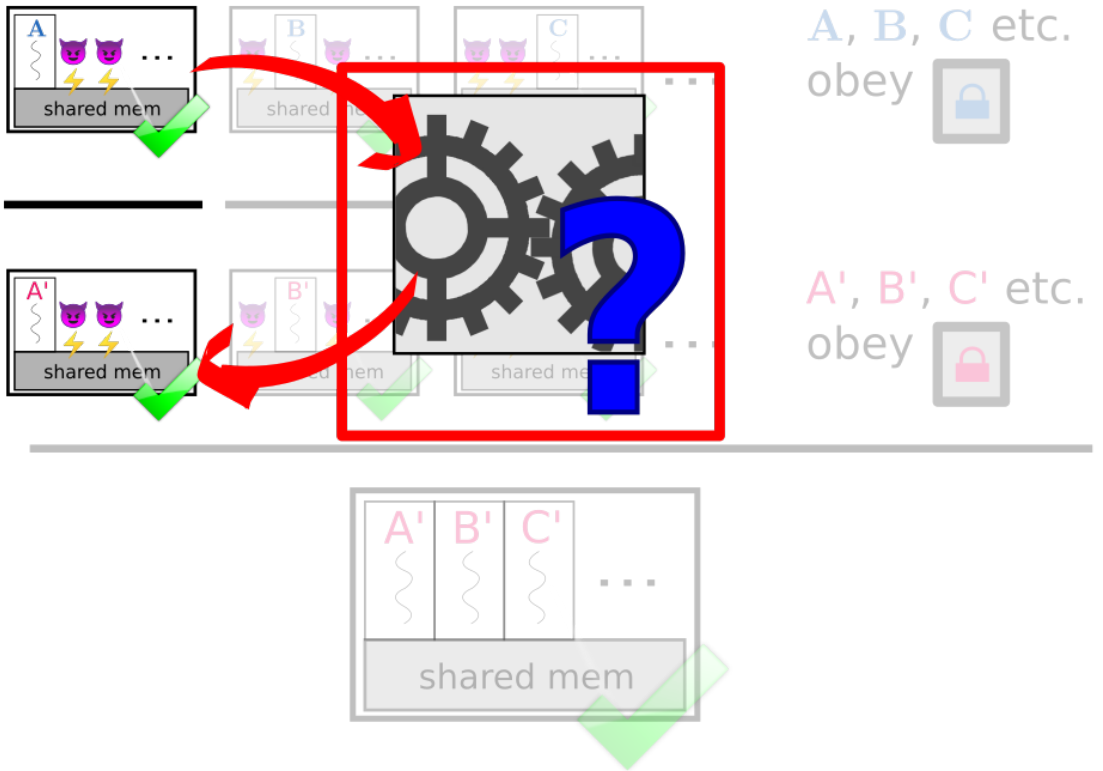
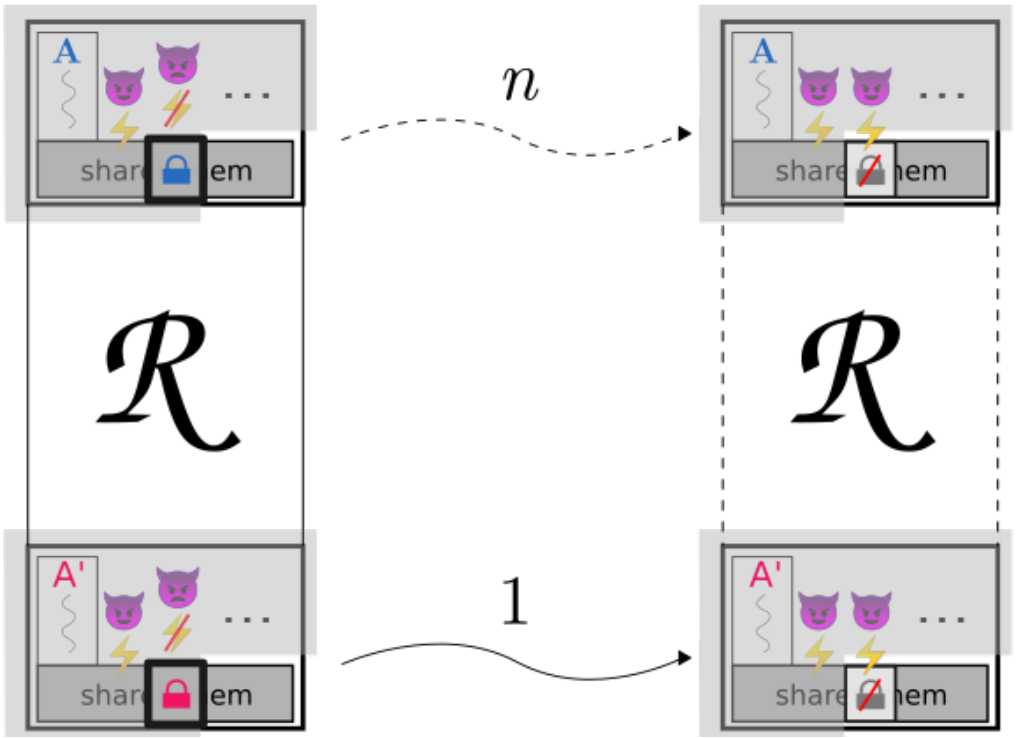


Compiler verification

Per-thread *simpler compositional refinement* [Murray+, AFP], instantiated with $\mathcal{R}$ characterising a compiler.

$\exists n \;.\; n =$ abs_steps A A'



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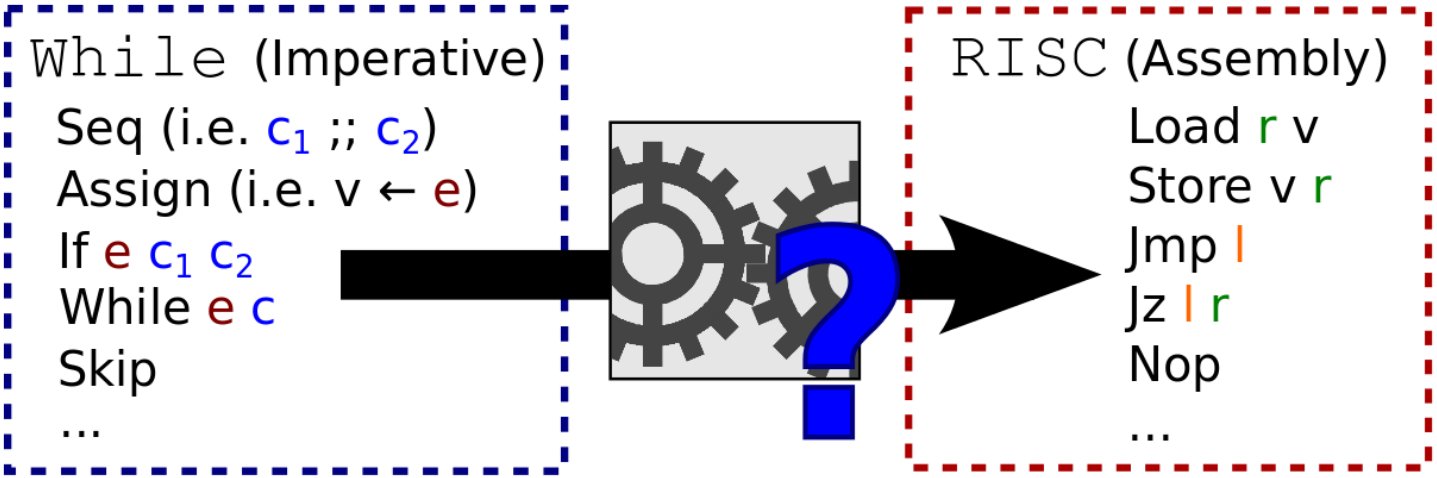
Proof of concept: a While-to-RISC compiler



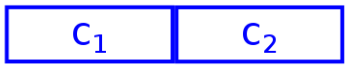
(Note: Constant-time execution steps, no cache effects)

Compiler verification

Per-thread *simpler compositional refinement* [Murray+, AFP], instantiated with $\mathcal{R}$ characterising a compiler.

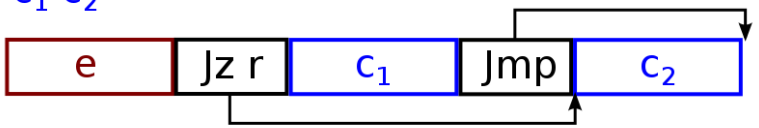
Proof of concept: a While-to-RISC compiler

- Seq (i.e. c_1 ;; c_2)

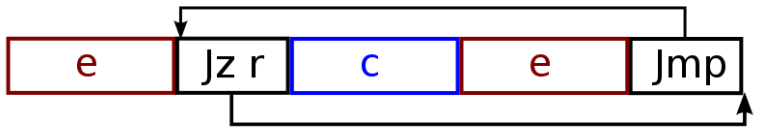


- Assign (i.e. v ← e)

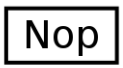
- If e c_1 c_2



- While e c



- Skip



~~- LockAcq l~~

~~- LockRel l~~

Based on *Fault-Resilient Non-interference* [Tedesco et al, 2016].

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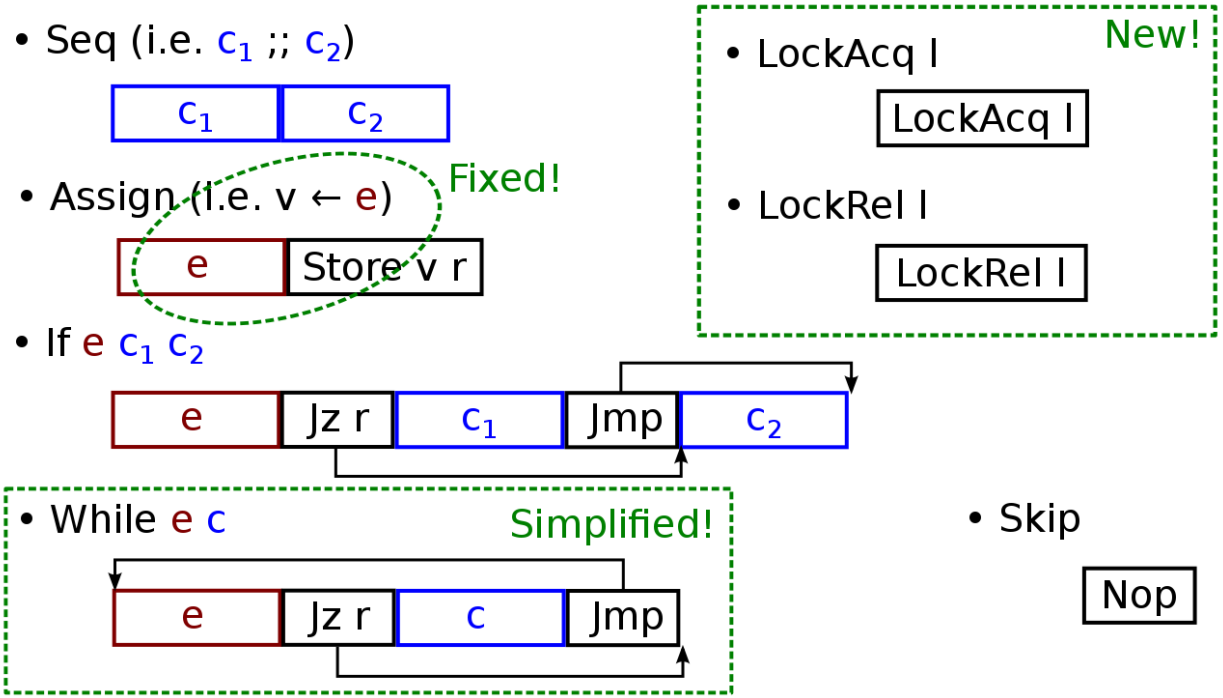
Proof of concept: a While-to-RISC compiler



Based on *Fault-Resilient Non-interference* [Tedesco et al, 2016].
Implemented in Isabelle/HOL, executable, verified.

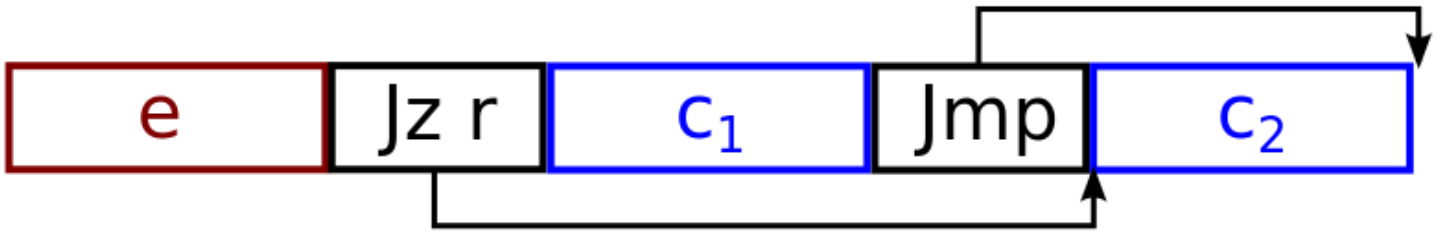
Compiler verification

Per-thread *simpler compositional refinement* [Murray+, AFP], instantiated with $\mathcal{R}$ characterising a compiler.

Proof of concept: a While-to-RISC compiler

e.g. $\mathcal{R}$ cases for If construct

If e c_1 c_2



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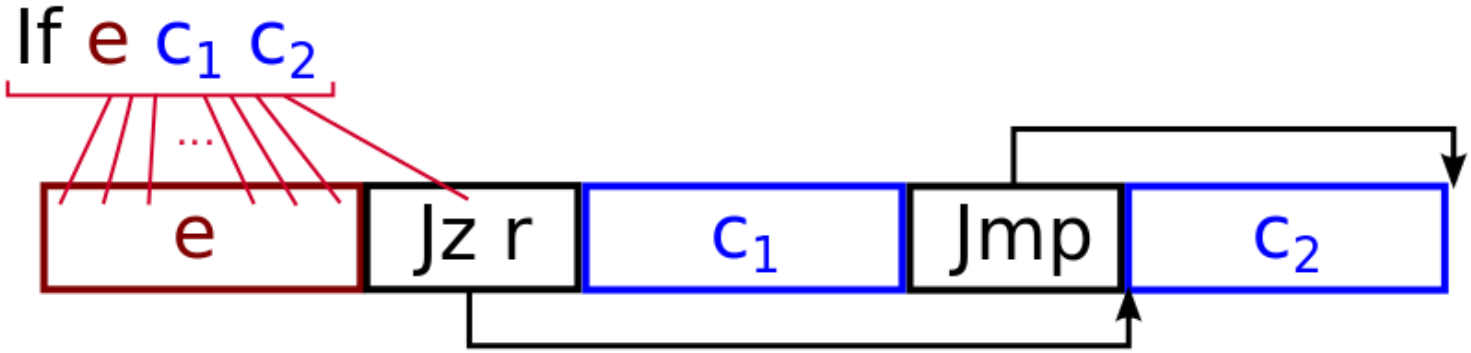

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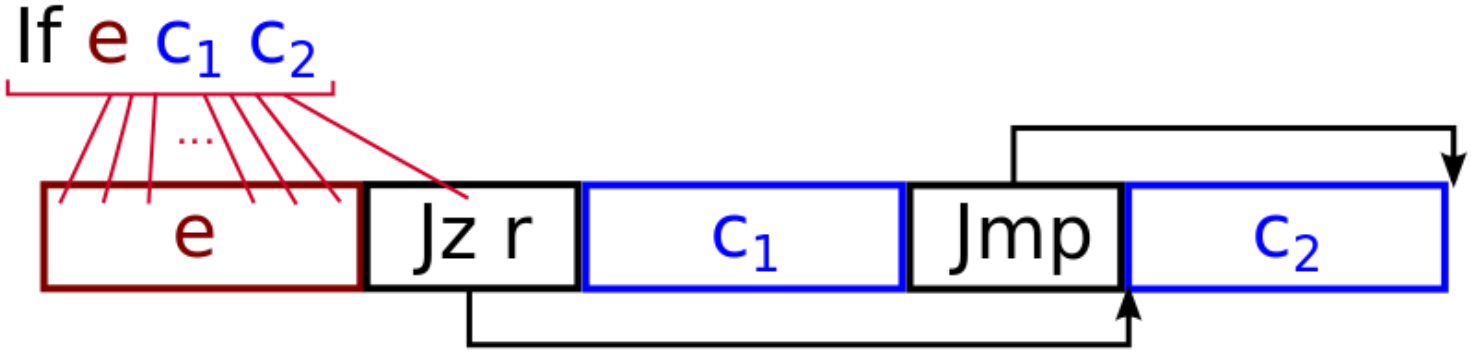

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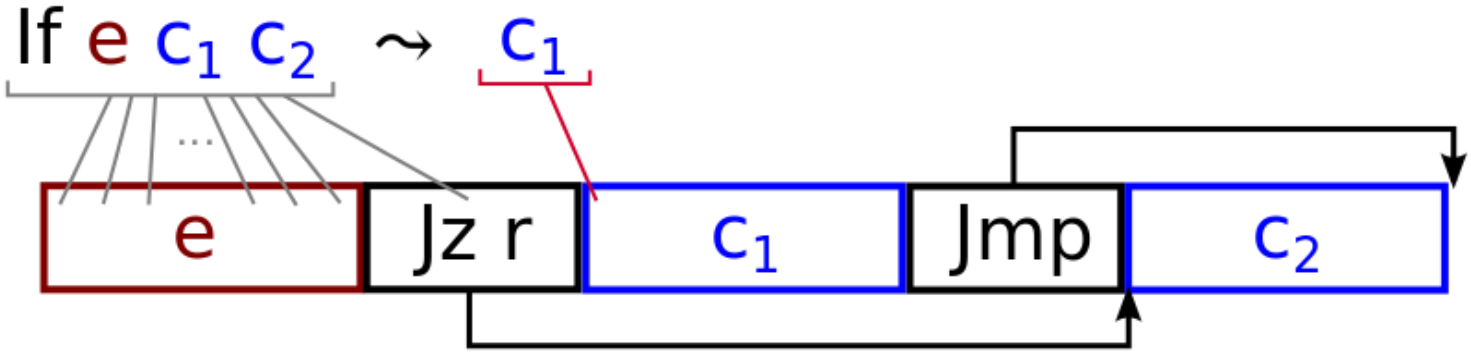

Relation is inductive for smaller program pairs c_1, c_2

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Per-thread *simpler compositional refinement* [Murray+, AFP], instantiated with $\mathcal{R}$ characterising a compiler.

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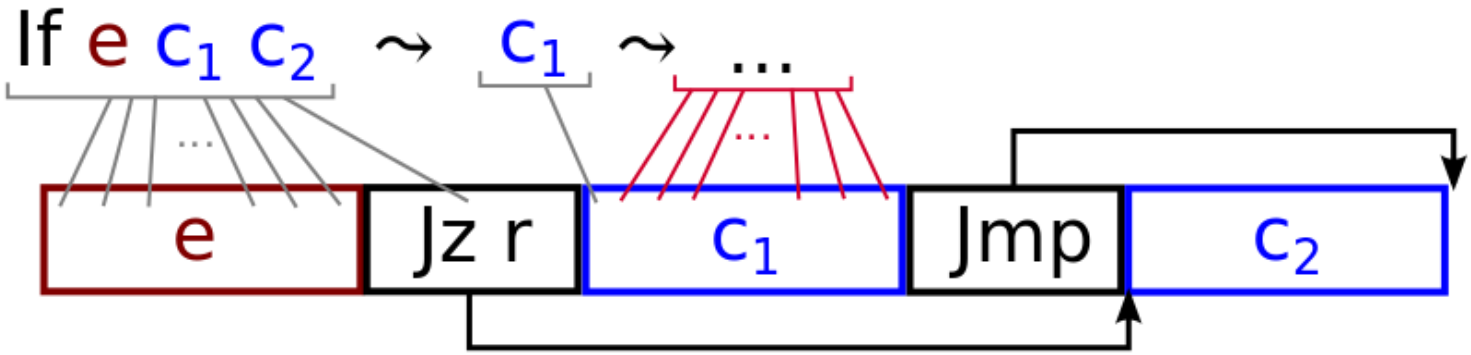

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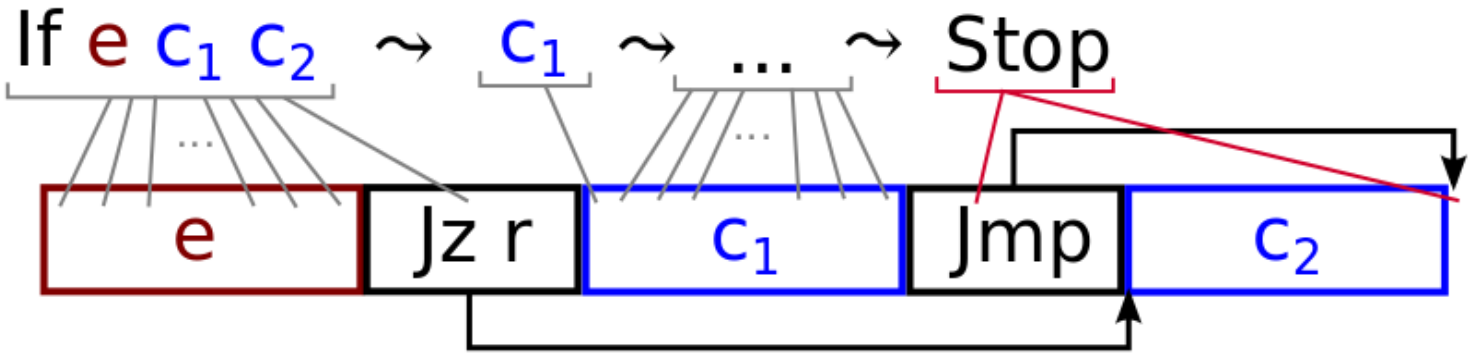

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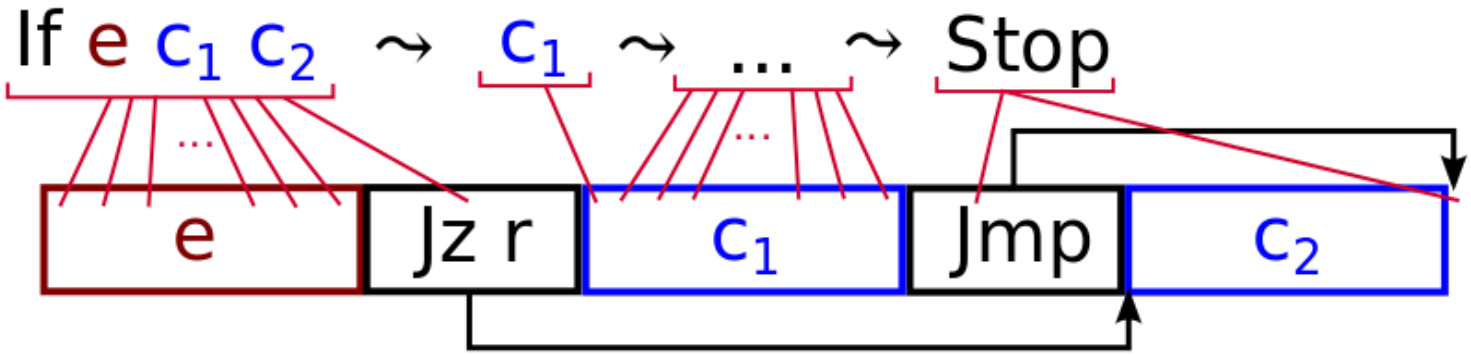

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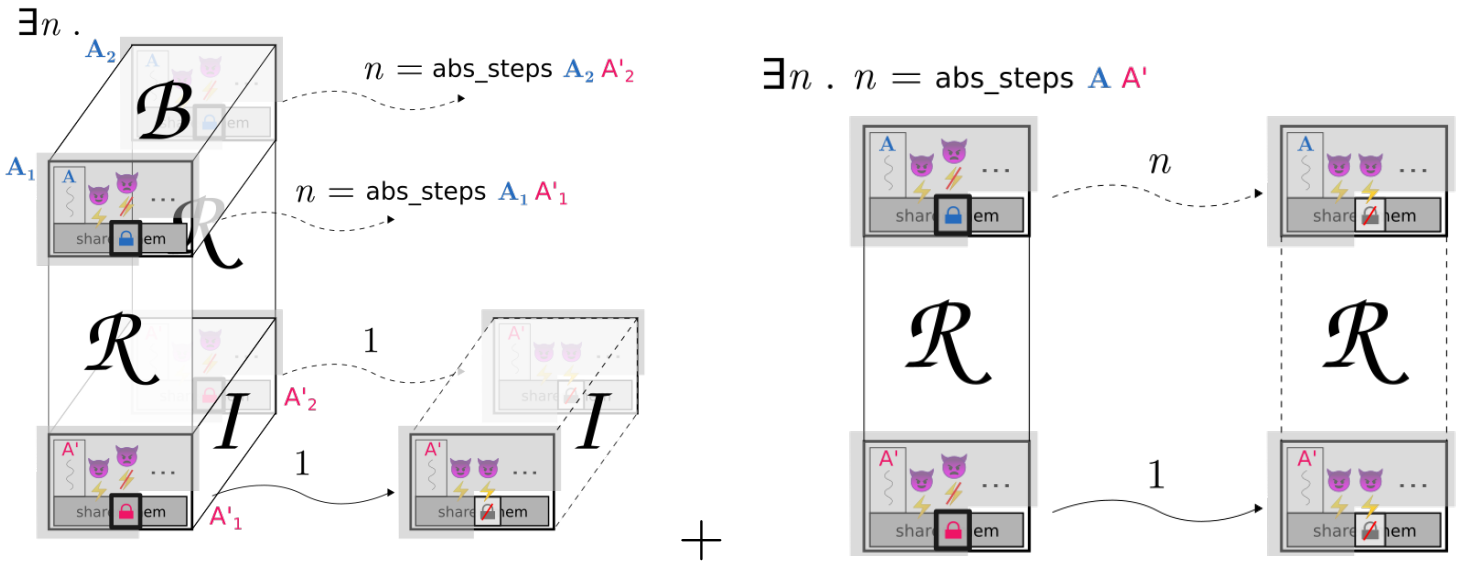

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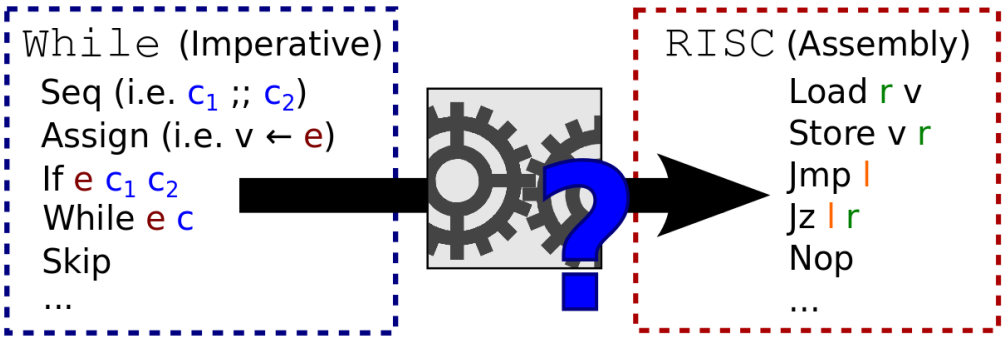
- Theorem: Compiler input is related to its output by $\mathcal{R}$
  - Started with same observable initial state.
  - No branching on H values. (Same as for type system.)



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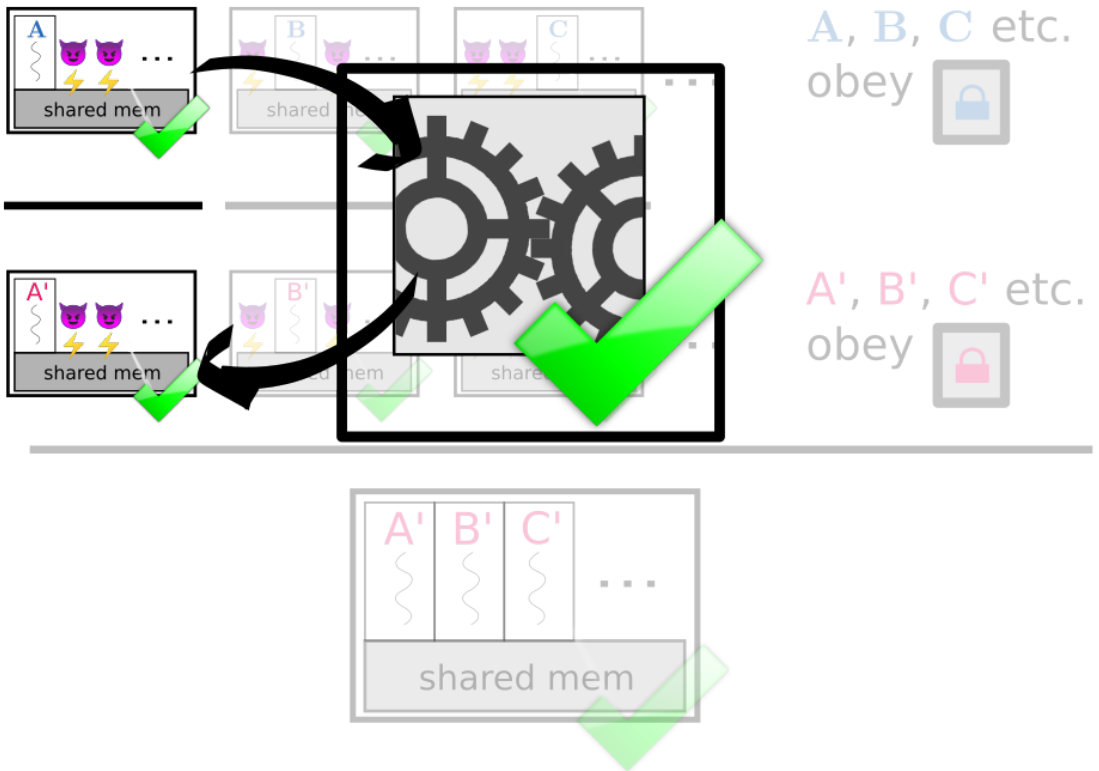

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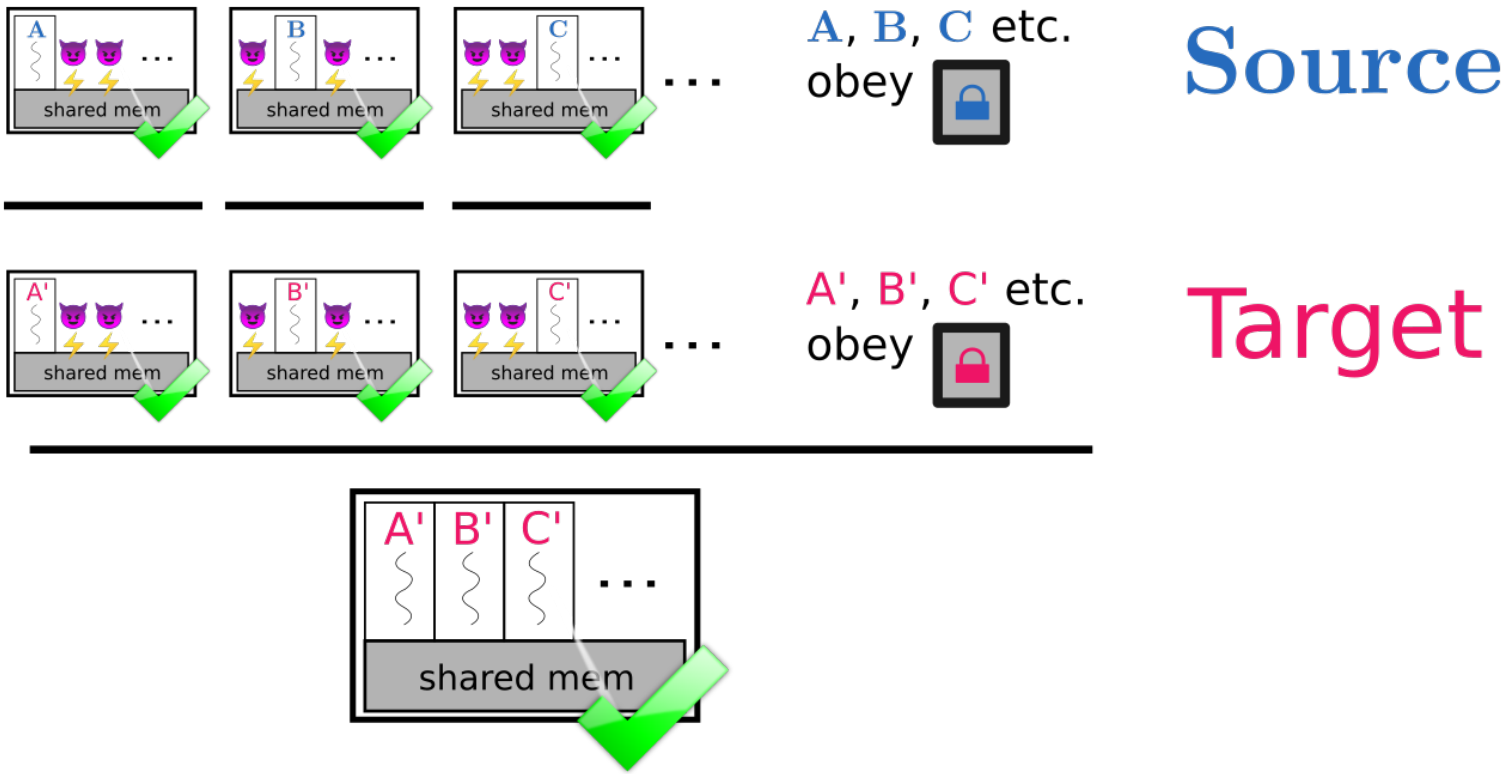

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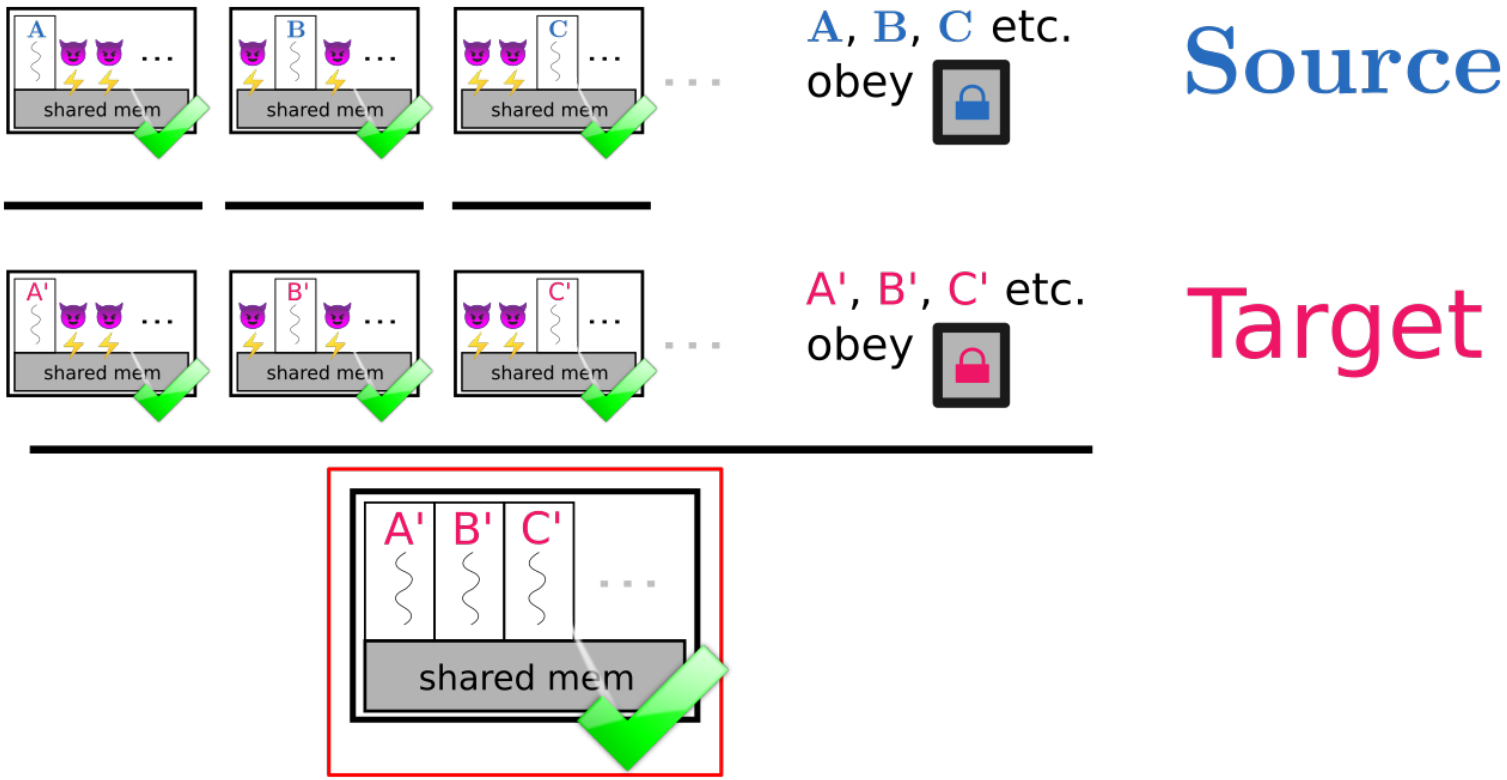

Exercised on verified Cross Domain Desktop Compositor model.

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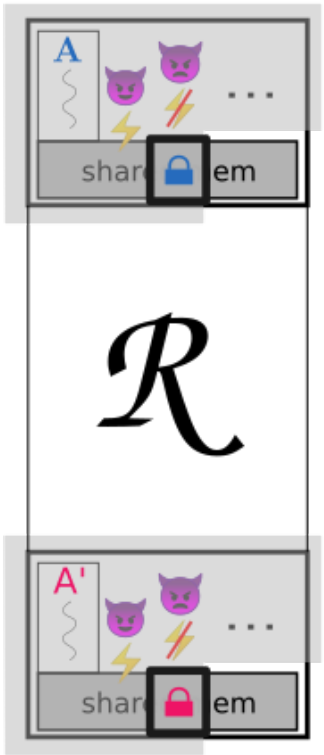

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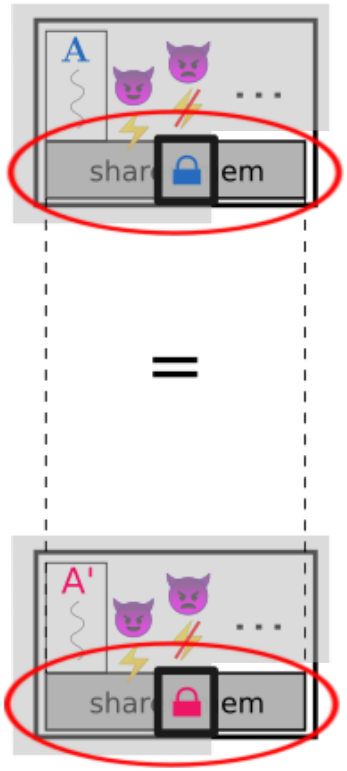

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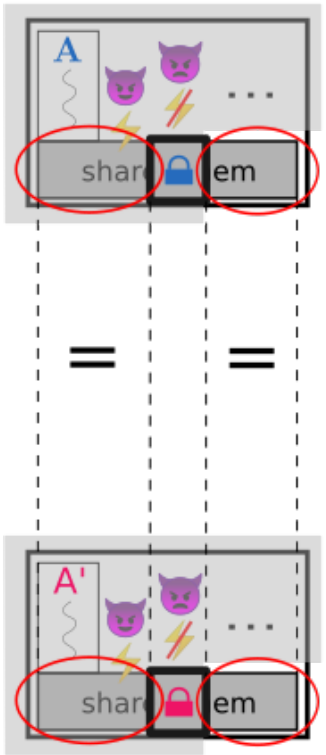

Relax for shared memory out of reach of attacker model?

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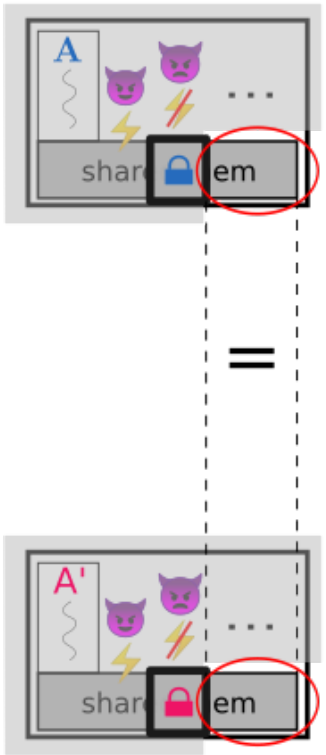

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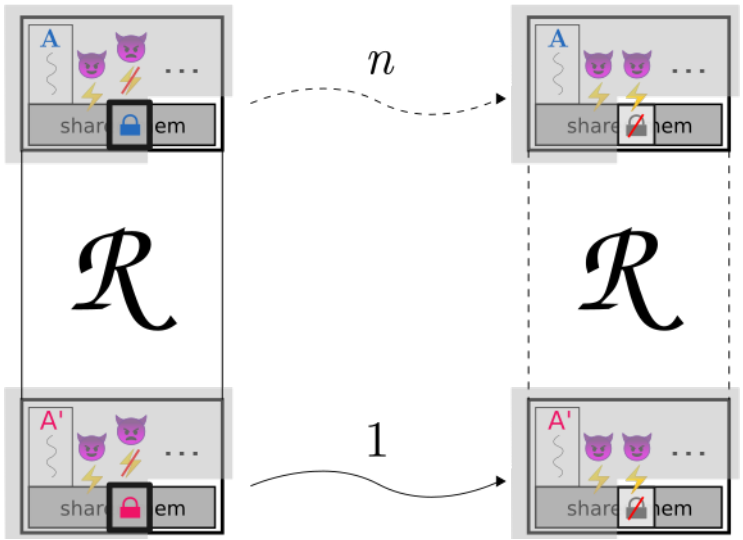

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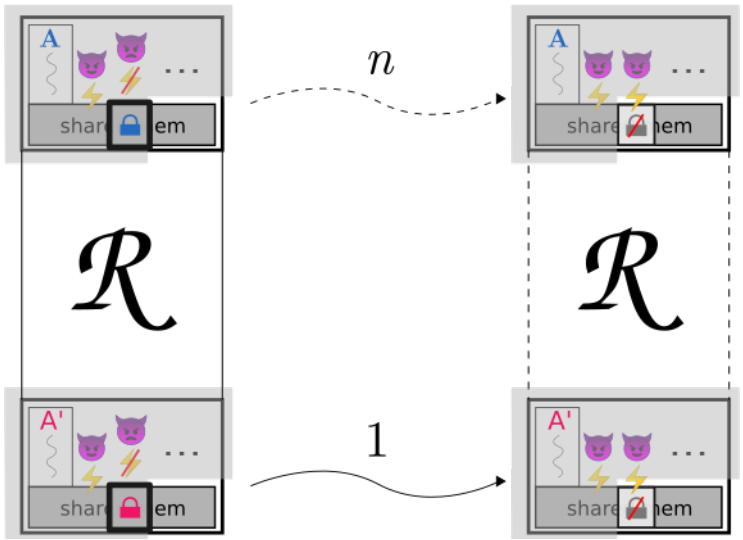

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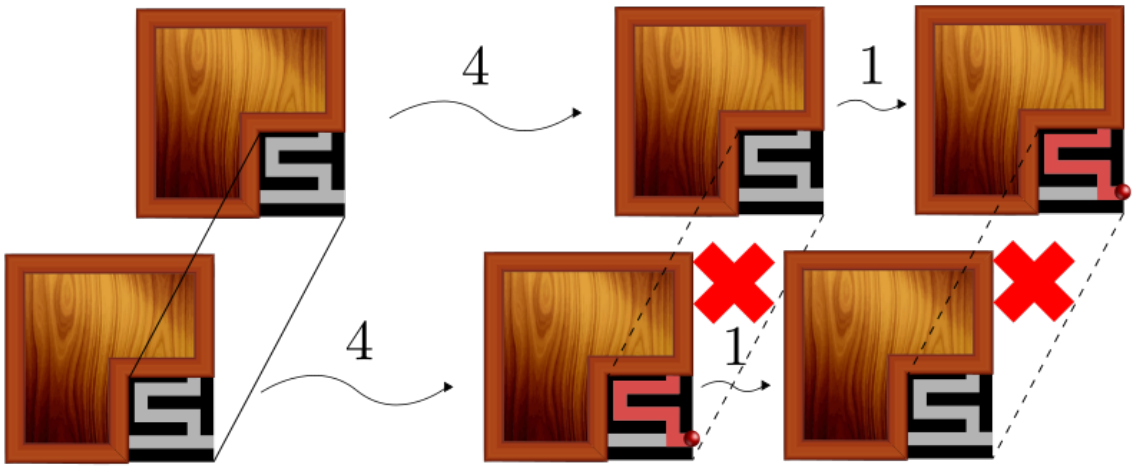

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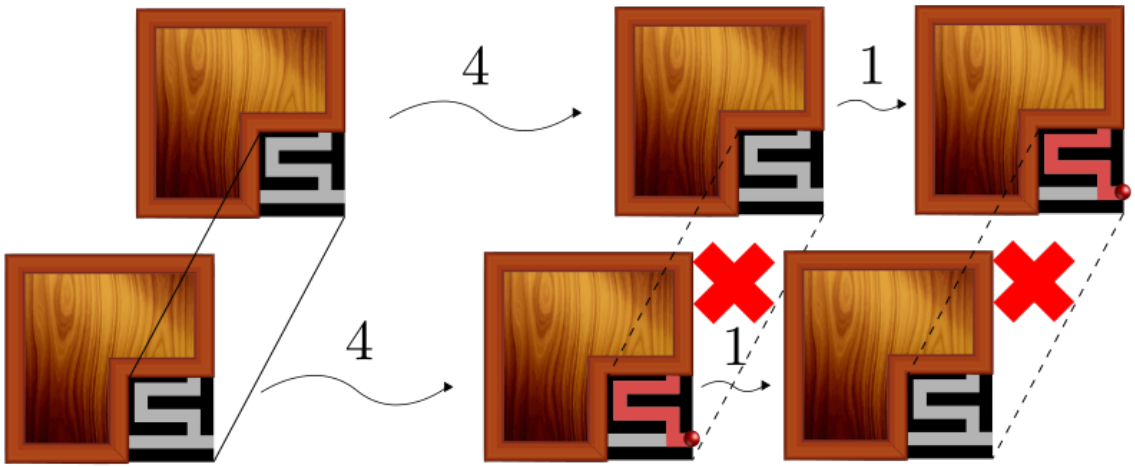

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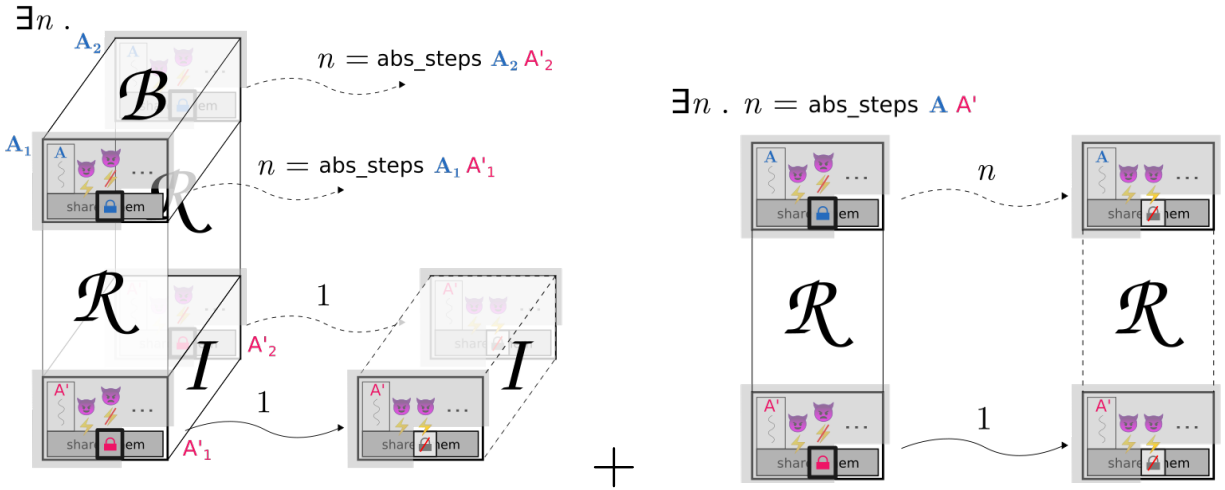

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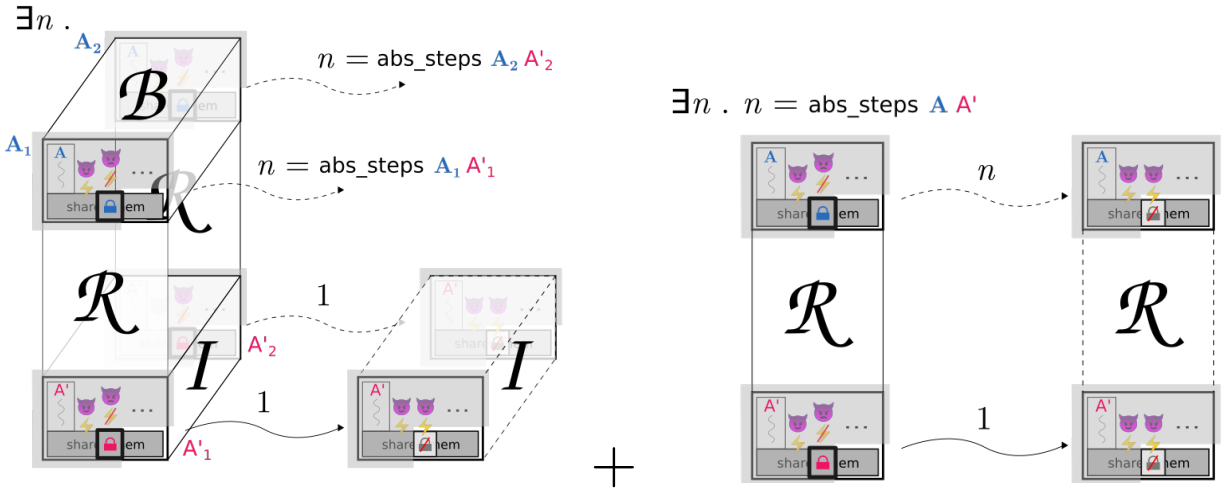
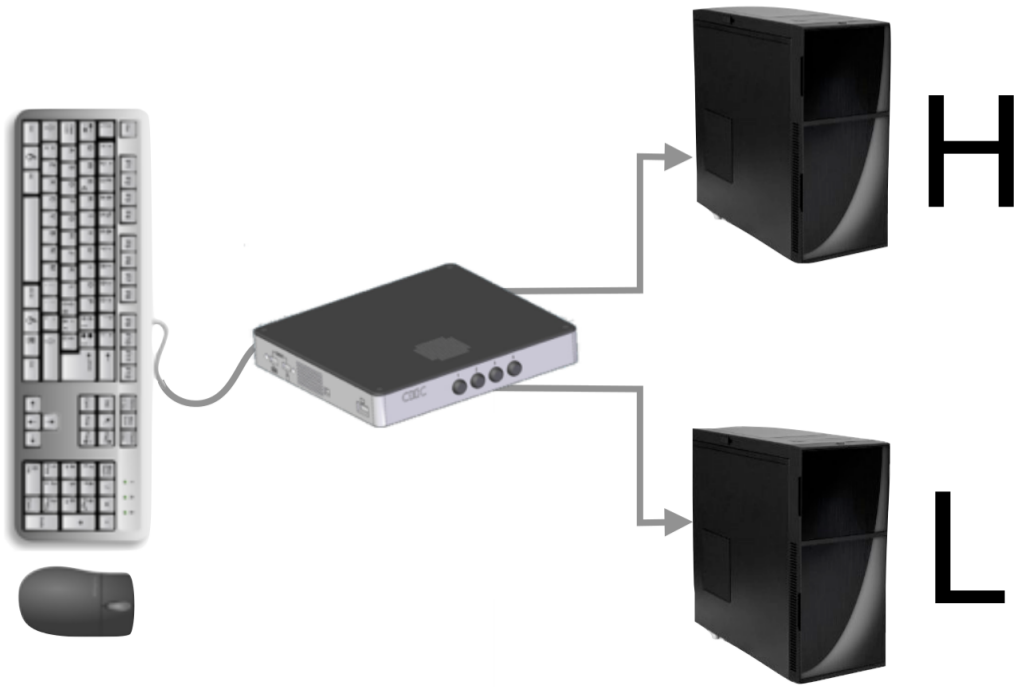


Thank you! Q & A

Appendix: Co-habiting attacker?

CDDC case study, again.



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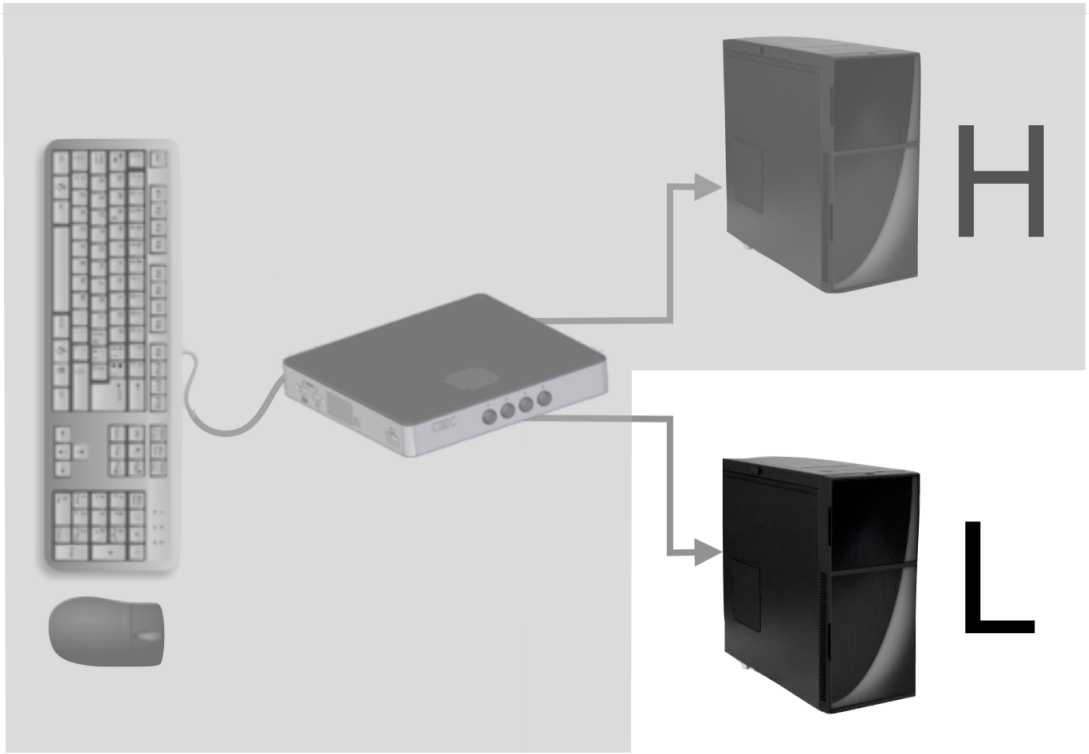

Untrusted sink: input device event stream out to Low machine.

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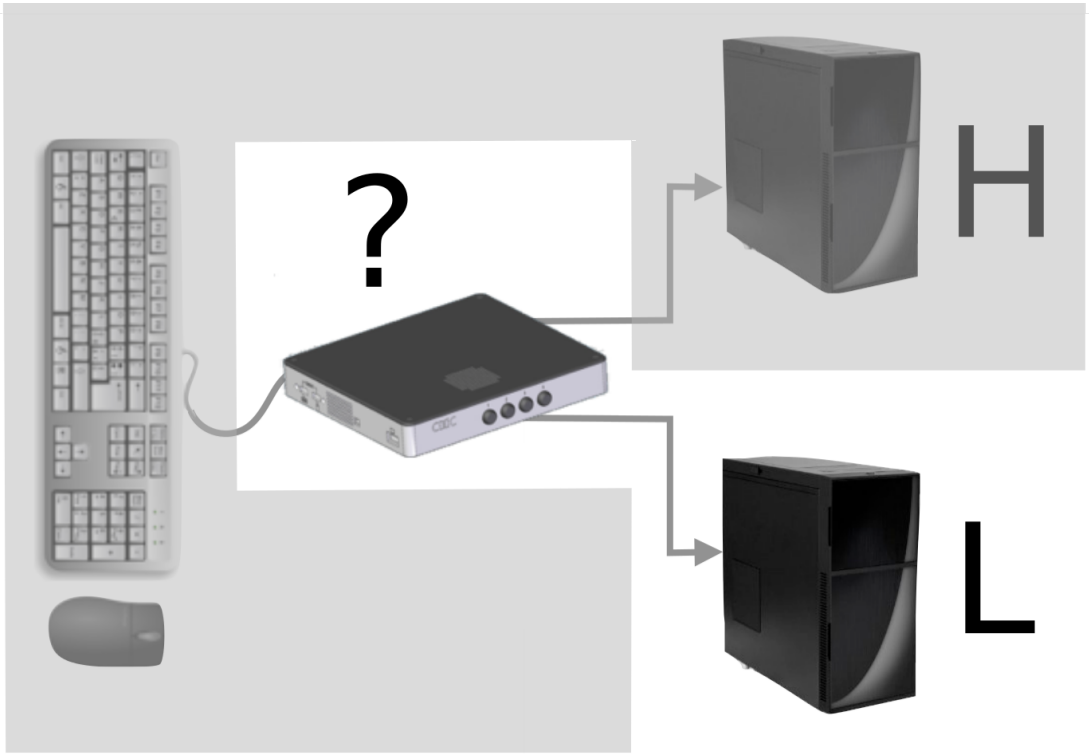

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What else can we afford to distrust?

Appendix: Co-habiting attacker?

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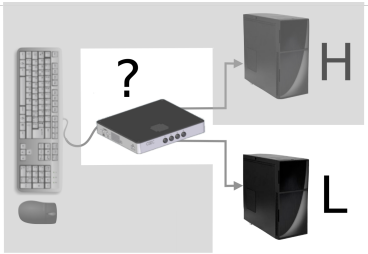
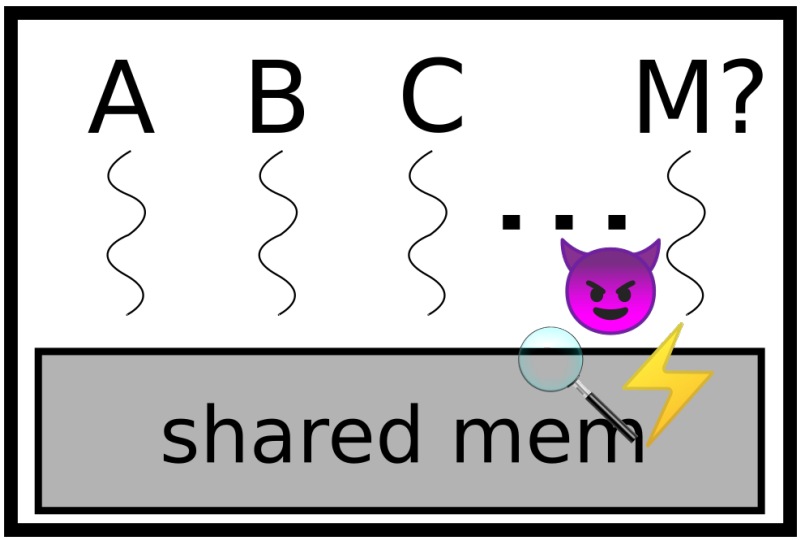


Hypothetically, a co-habiting "attacker"...?



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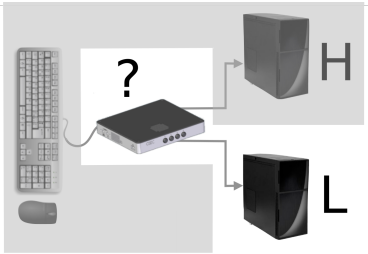

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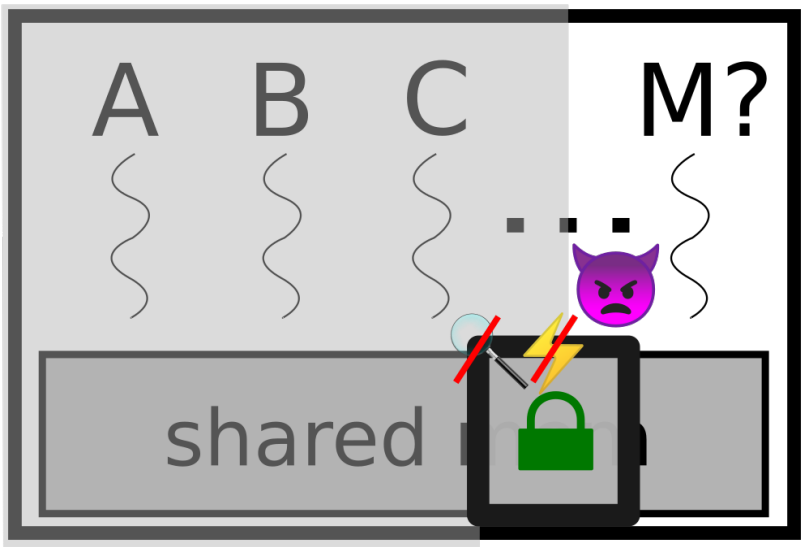

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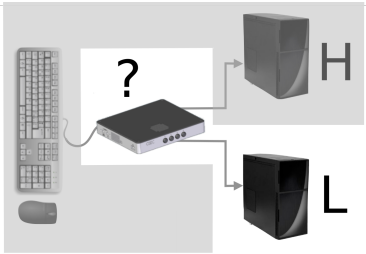

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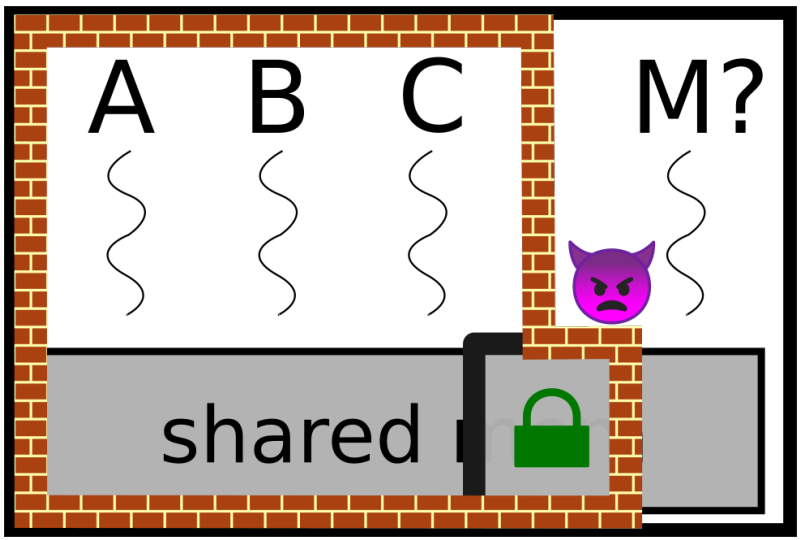


... if it in fact cannot see/touch High nor locked part of state.
This may be reasonable in, e.g. a separation kernel environment.

Appendix: "Simpler" refinement

No H-branching ("L-shaped") obligation:

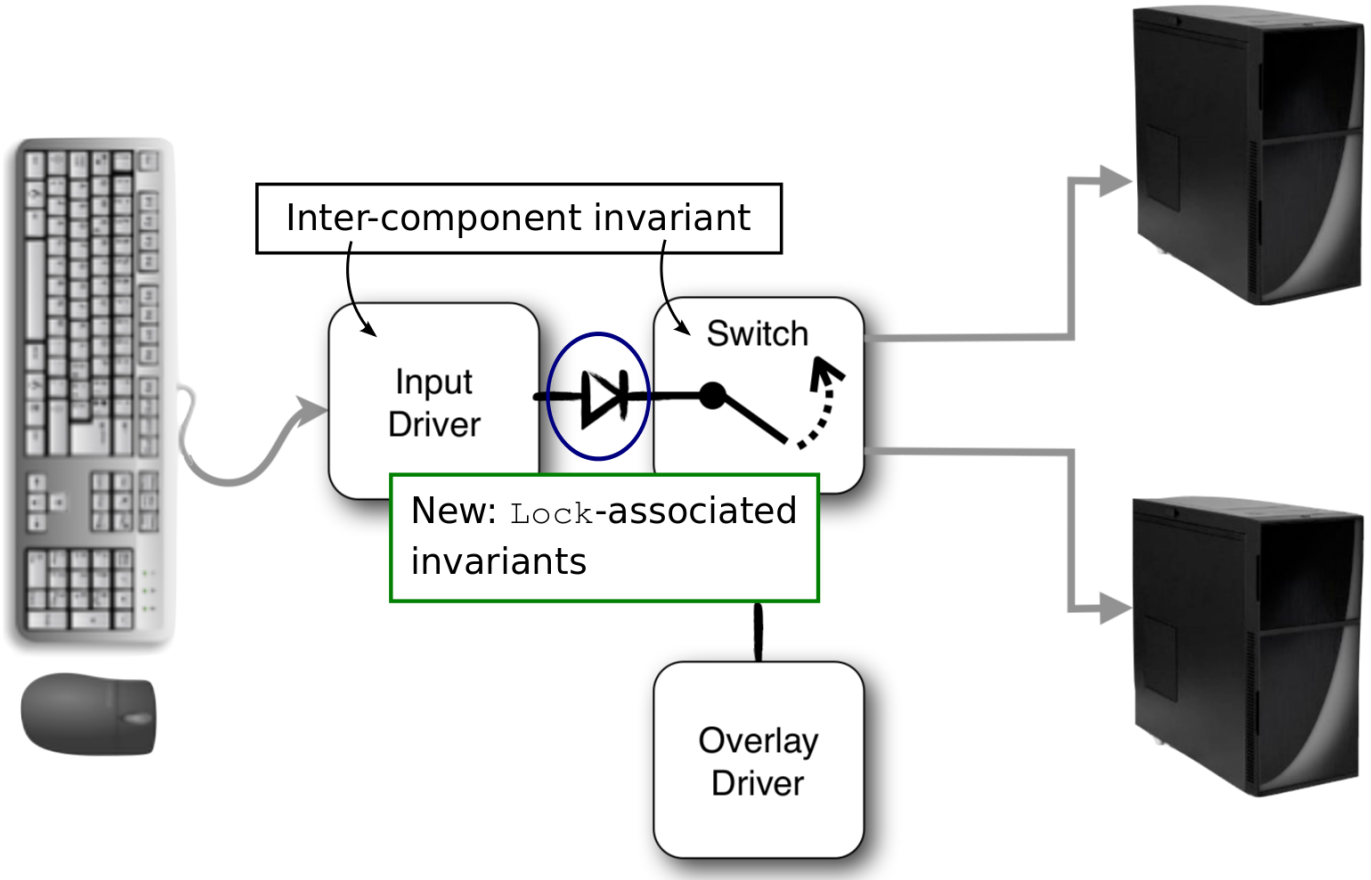
```
definition
  simpler_refinement_safe
where
  "simpler_refinement_safe R_A R P abs_steps ≡
  ∀c_1A mds_A mem_1A c_2A mem_2A c_1C mds_C mem_1C c_2C mem_2C. (⟨c_1A,mds_A,mem_1A⟩_A,⟨c_2A,mds_A,mem_2A⟩_A) ∈ R_A ∧
      (⟨c_1A,mds_A,mem_1A⟩_A,⟨c_1C, mds_C, mem_1C⟩_C) ∈ R ∧ (⟨c_2A,mds_A,mem_2A⟩_A,⟨c_2C, mds_C, mem_2C⟩_C) ∈ R ∧
       (⟨c_1C, mds_C, mem_1C⟩_C, ⟨c_2C, mds_C, mem_2C⟩_C) ∈ P  ⟶
           (stops_C ⟨c_1C, mds_C, mem_1C⟩_C = stops_C ⟨c_2C, mds_C, mem_2C⟩_C) ∧
           (abs_steps ⟨c_1A,mds_A,mem_1A⟩_A ⟨c_1C, mds_C, mem_1C⟩_C = abs_steps ⟨c_2A,mds_A,mem_2A⟩_A ⟨c_2C, mds_C, mem_2C⟩_C) ∧
           (∀mds_1C' mds_2C' mem_1C' mem_2C' c_1C' c_2C'. ⟨c_1C, mds_C, mem_1C⟩_C ⇝_C ⟨c_1C', mds_1C', mem_1C'⟩_C  ∧
                                                  ⟨c_2C, mds_C, mem_2C⟩_C ⇝_C ⟨c_2C', mds_2C', mem_2C'⟩_C ⟶
                                                  (⟨c_1C', mds_1C', mem_1C'⟩_C, ⟨c_2C', mds_2C', mem_2C'⟩_C) ∈ P ∧
                                                  mds_1C' = mds_2C')"
```

Provisos and simulation relation:

```
definition
  secure_refinement_simpler
where
  "secure_refinement_simpler R_A R P abs_steps ≡
  closed_others R ∧
  preserves_modes_mem R ∧
  new_vars_private R ∧
  simpler_refinement_safe R_A R P abs_steps ∧
  conc.closed_glob_consistent P ∧
  (∀ c_1A mds_A mem_1A c_1C mds_C mem_1C.
   (⟨ c_1A, mds_A, mem_1A ⟩_A, ⟨ c_1C, mds_C, mem_1C ⟩_C) ∈ R ⟶
    (∀ c_1C' mds_C' mem_1C'. ⟨ c_1C, mds_C, mem_1C ⟩_C ⇝_C ⟨ c_1C', mds_C', mem_1C' ⟩_C ⟶
     (∃ c_1A' mds_A' mem_1A'. abs.neval ⟨ c_1A, mds_A, mem_1A ⟩_A (abs_steps ⟨c_1A,mds_A,mem_1A⟩_A ⟨c_1C,mds_C,mem_1C⟩_C) ⟨ c_1A', mds_A', mem_1A' ⟩_A ∧
                   (⟨ c_1A', mds_A', mem_1A' ⟩_A, ⟨ c_1C', mds_C', mem_1C' ⟩_C) ∈ R)))"
```

(See: `https://www.isa-afp.org/entries/Dependent_SIFUM_Refinement.html`)

Appendix: CDDC 3-component architecture verification



Invariant on integrity of Switch's internal state w.r.t. indicator.
To appear: EuroS&P'18.