



Time Protection: The Missing OS Abstraction

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UNSW
SYDNEY



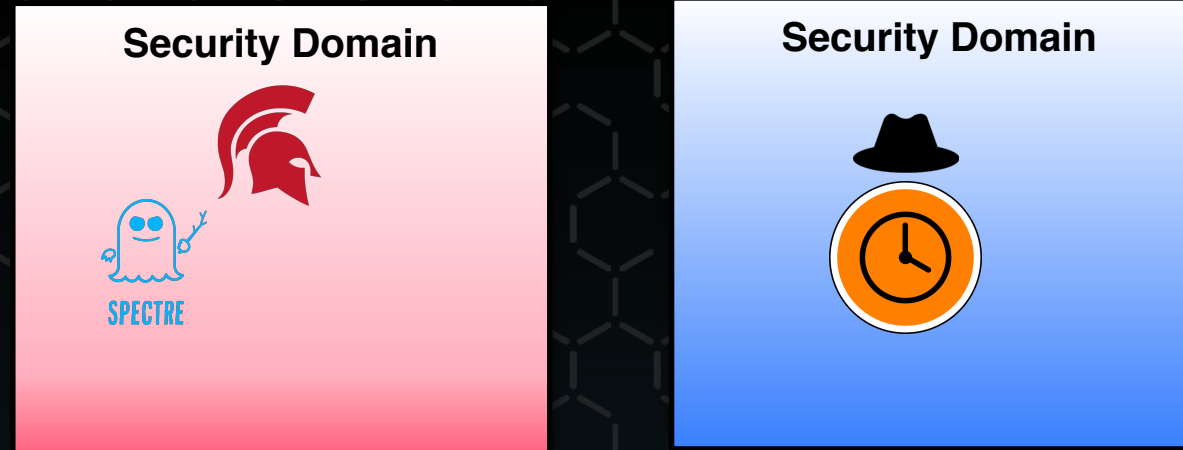
THE UNIVERSITY
of ADELAIDE



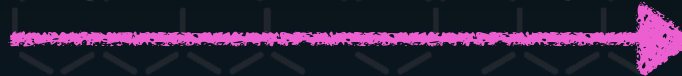
UNIVERSITY OF
BIRMINGHAM



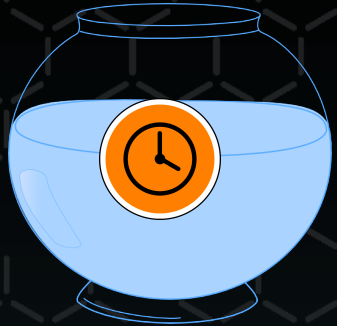
Enforcing time protection at the OS level



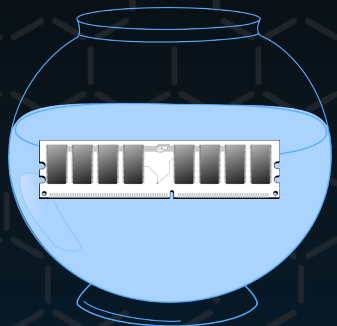
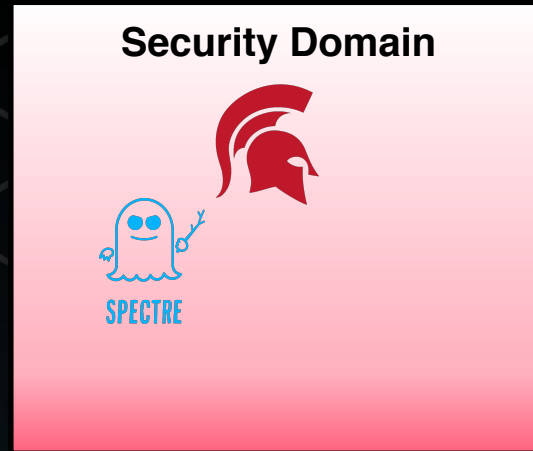
Sending information through timing



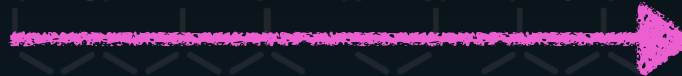
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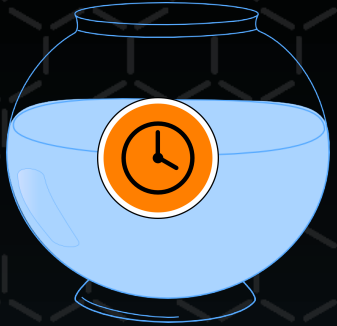
Security
Domain



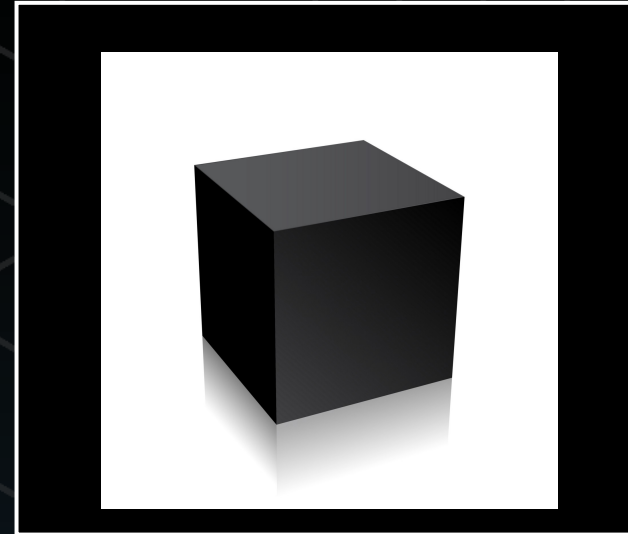
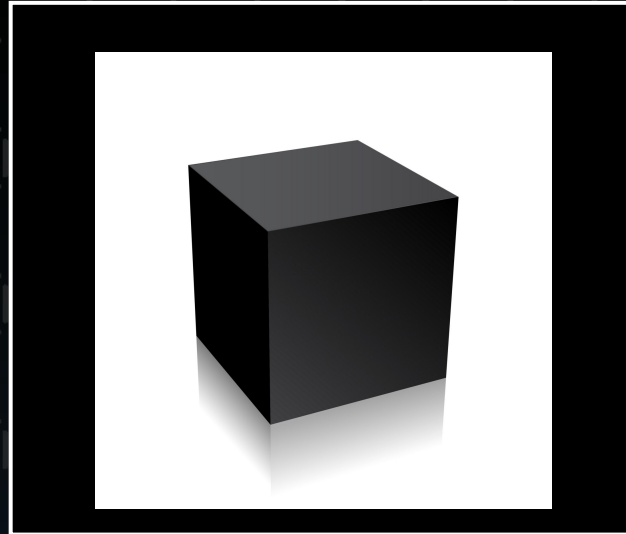
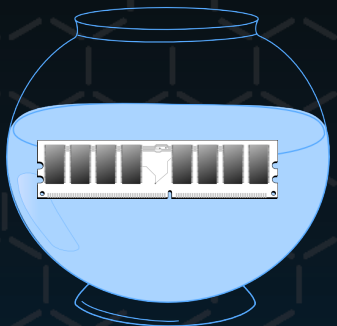
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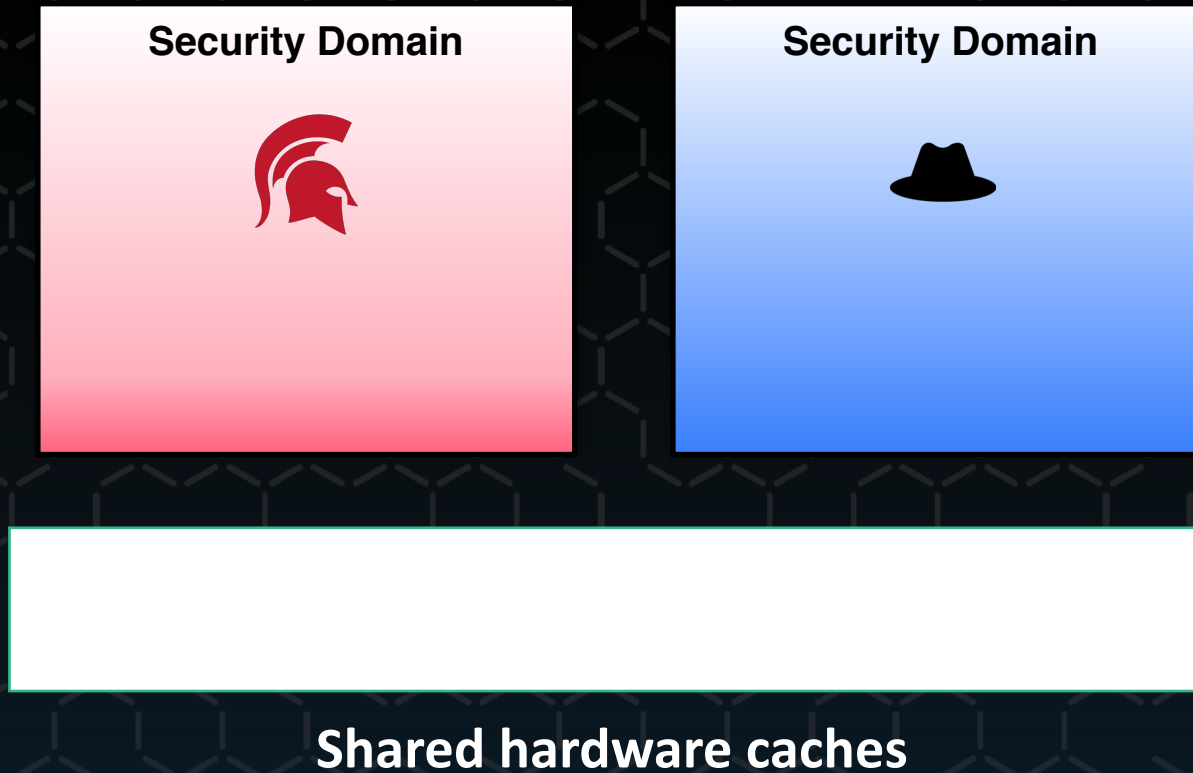
seconds
microseconds



Sending information through timing

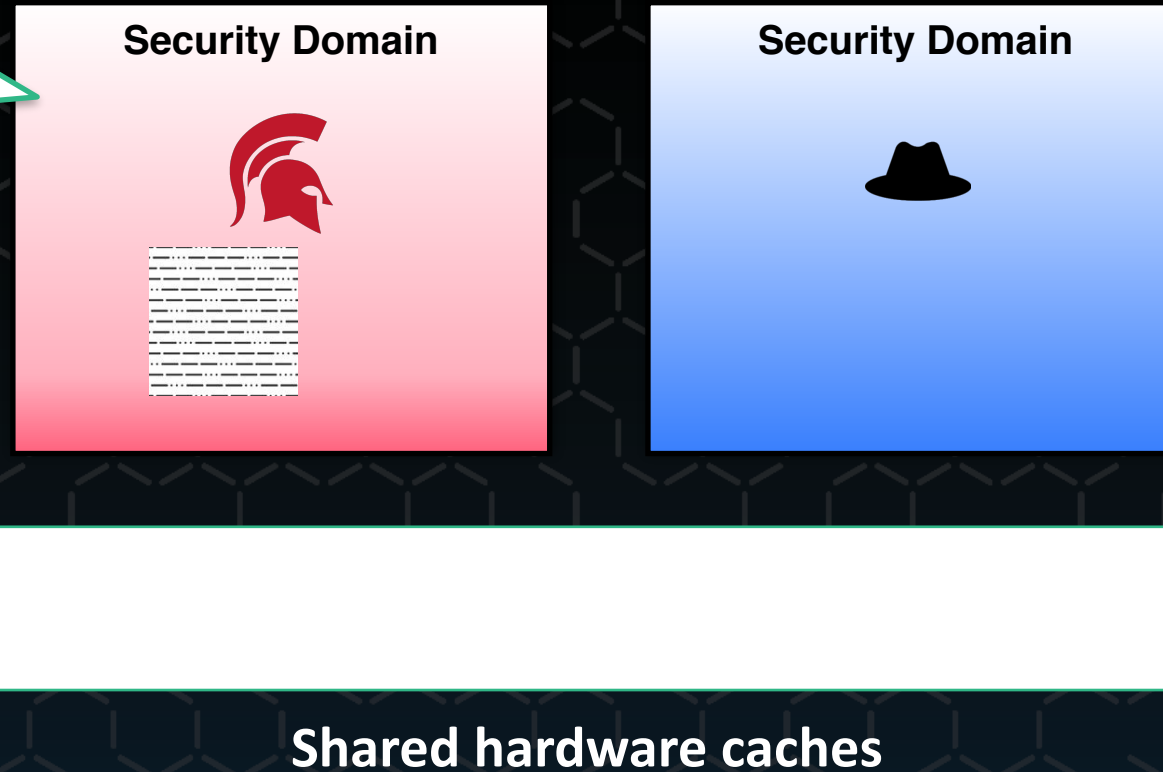


Microarchitectural Timing Channels



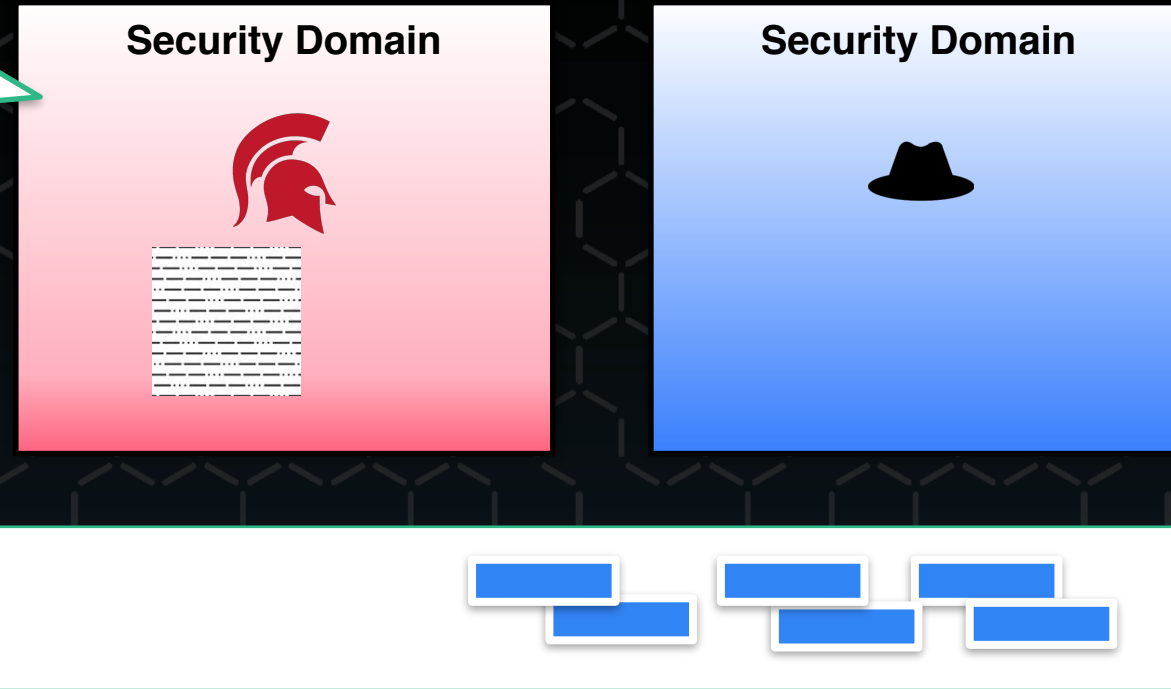
Microarchitectural Timing Channels

Welcome to Dresden



Microarchitectural Timing Channels

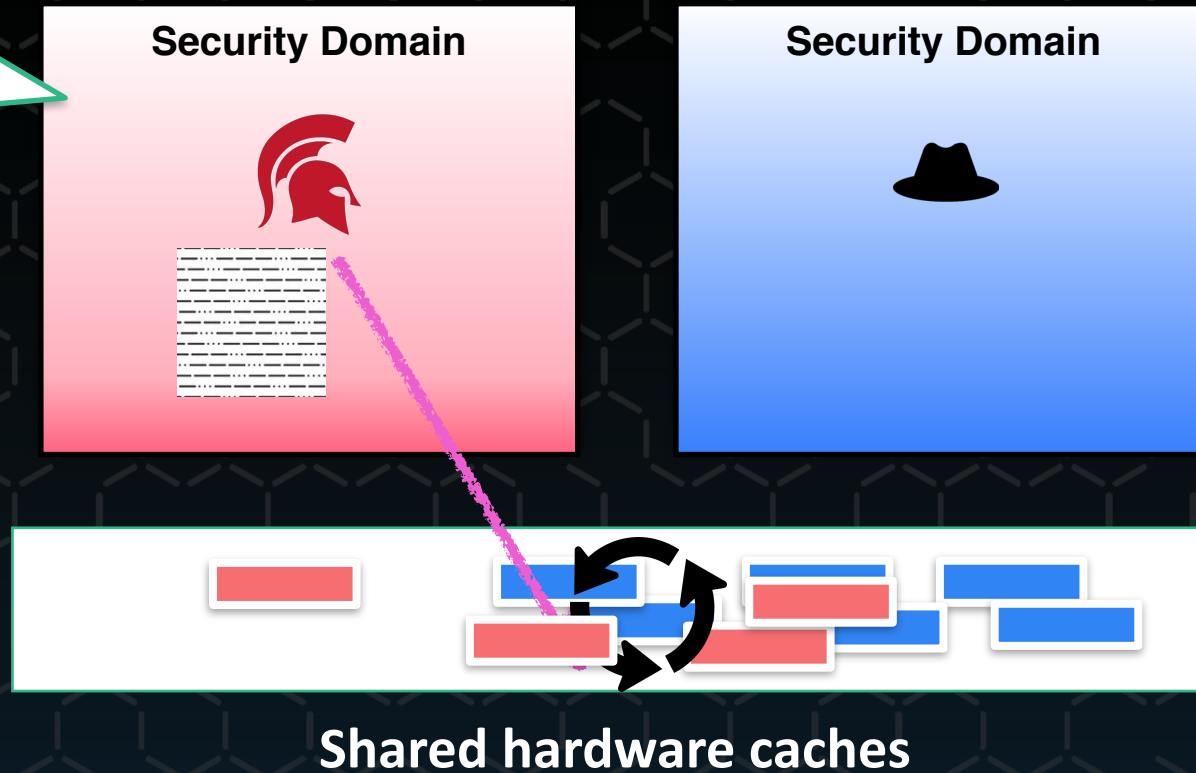
Welcome to Dresden



Shared hardware caches

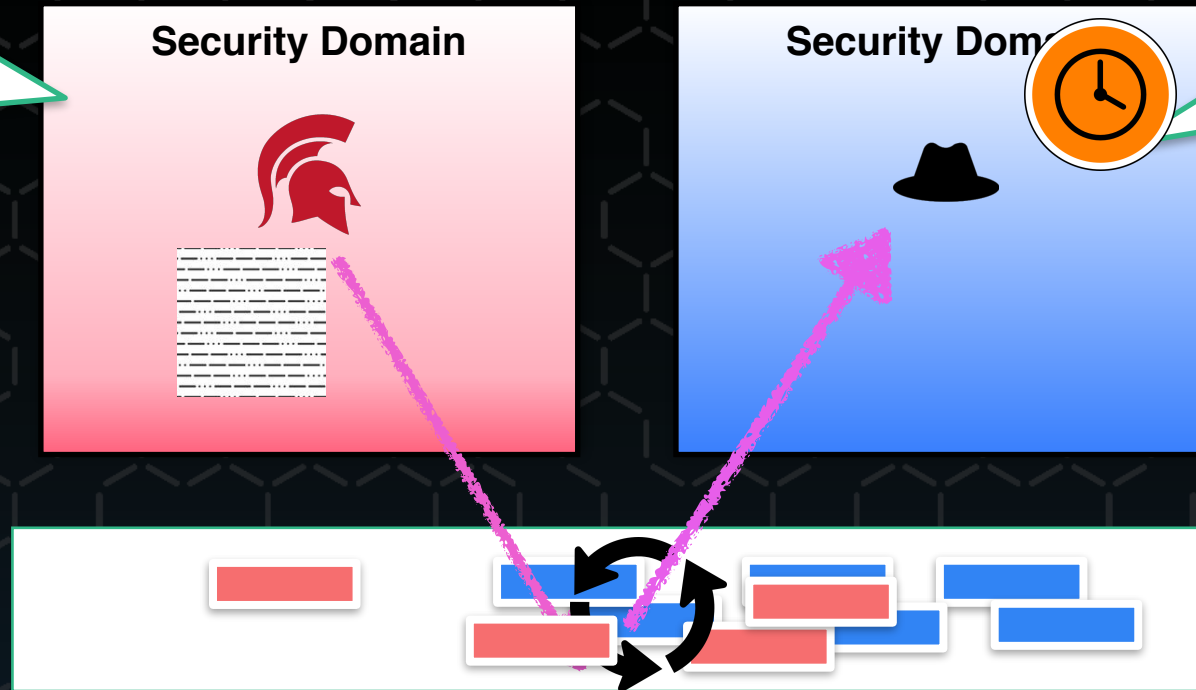
Microarchitectural Timing Channels

Welcome to Dresden



Microarchitectural Timing Channels

Welcome to Dresden

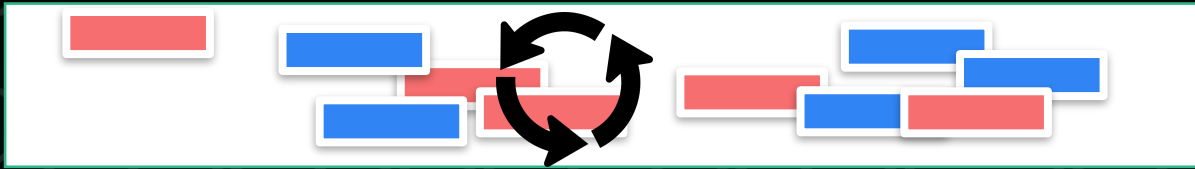


Fast Fast Slow Fast Fast
..... S F S FFF SSSS F

Not English,
but our
protocol...

Shared hardware caches

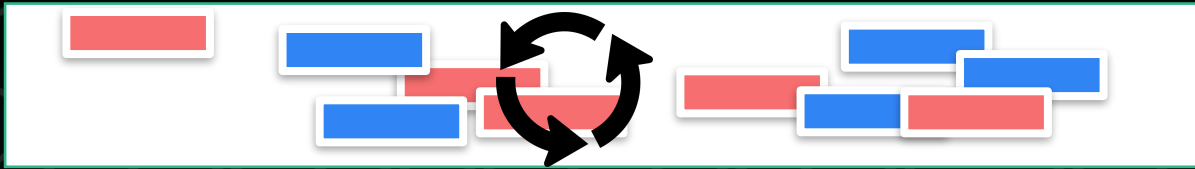
Contention, Contention, Contention...



Shared hardware caches

- Contention leaks information via timing
- Caches:
 - capacity-limited
 - stateful
- Resulting on temporal interference during:
 - time-shared access
 - concurrent access

Contention, Contention, Contention...

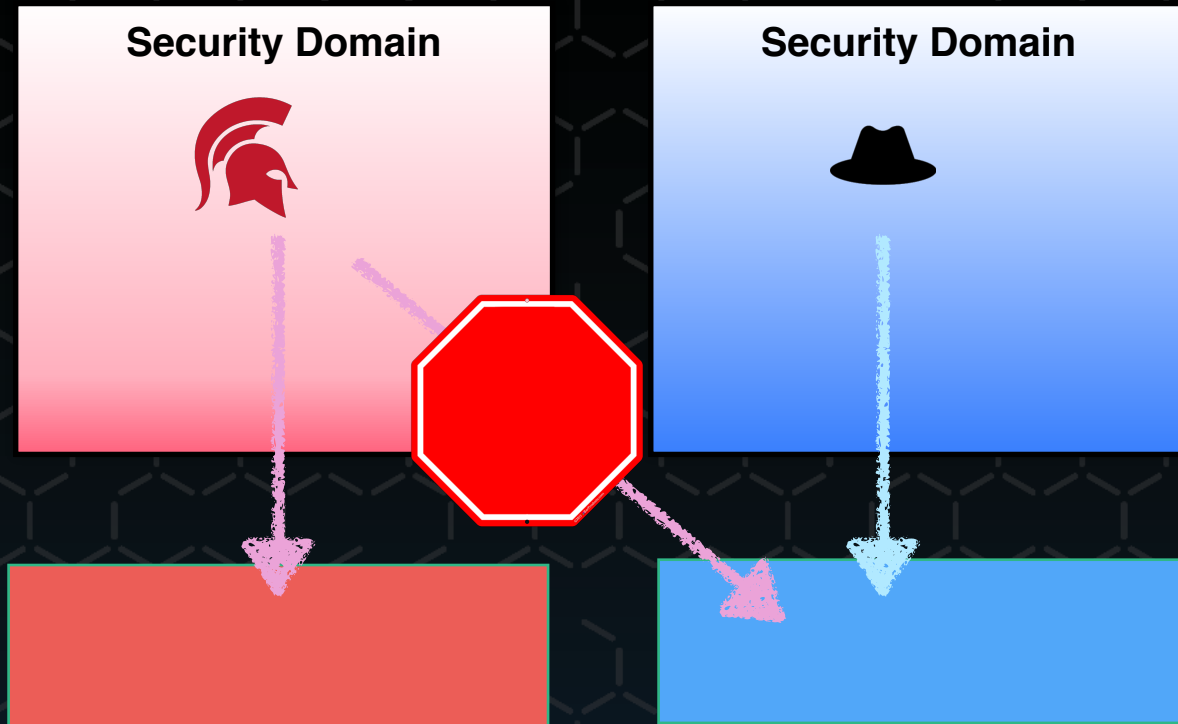


Shared hardware caches

Any state-holding microarchitectural feature:

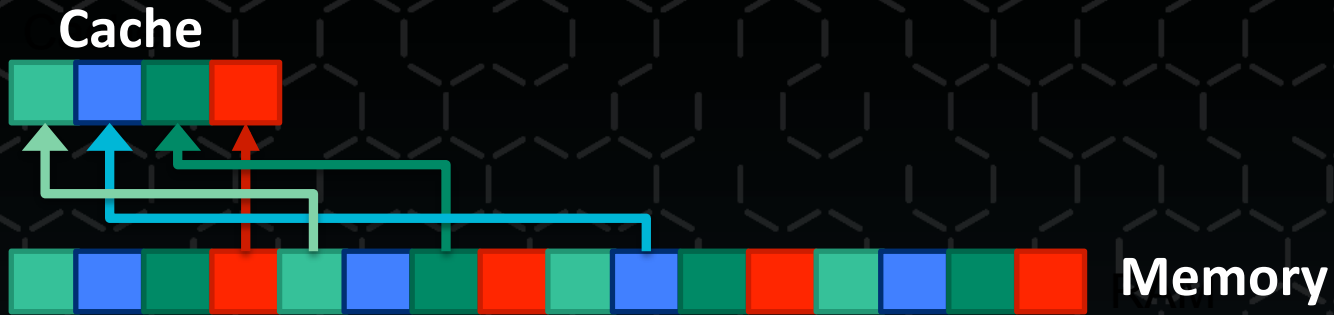
- Caches, branch predictor, TLB
- Contention leaks information via timing
- Caches:
 - capacity-limited
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Preventing Contention by Partitioning



Partitioned caches

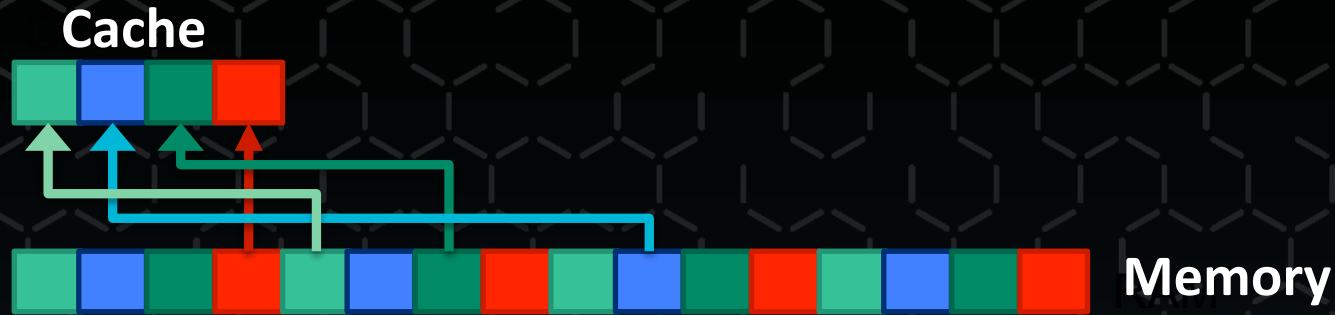
Spatial Partitioning



Cache colouring:

- Distributing coloured cache sets to coloured memory frames
- Memory management policy

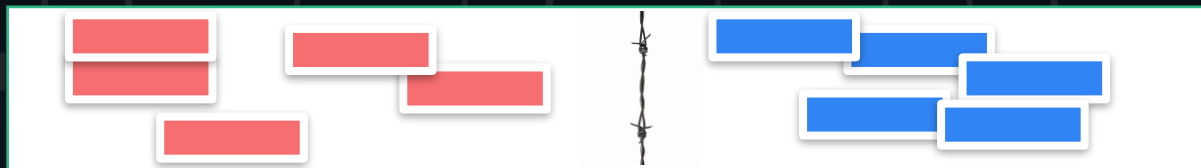
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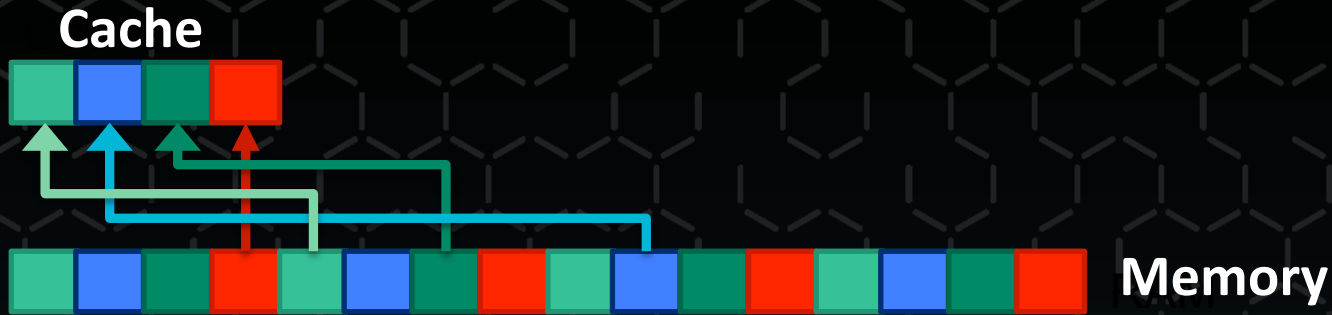
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Partition security domains on disjoint cache sets



Shared hardware caches

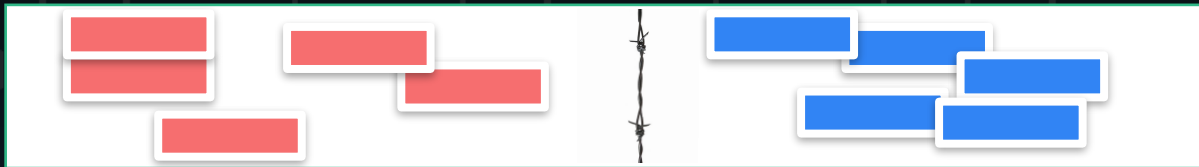
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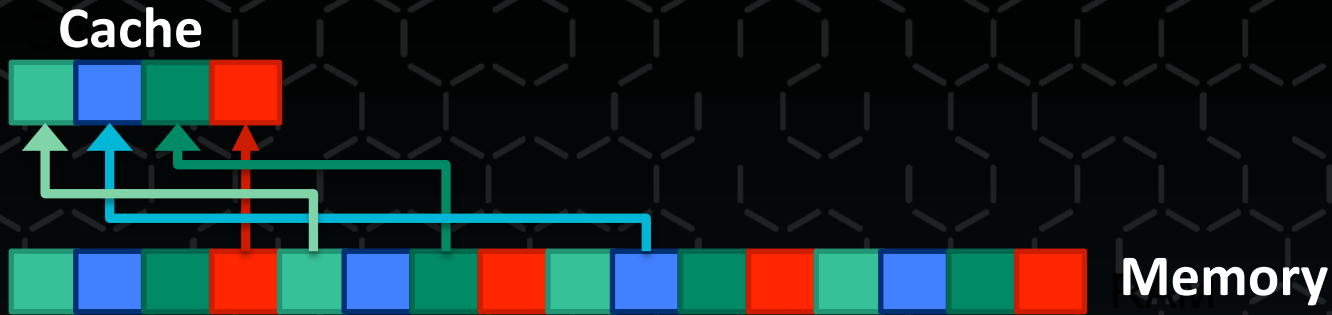
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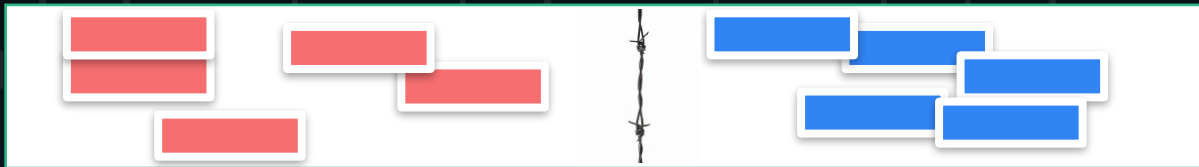
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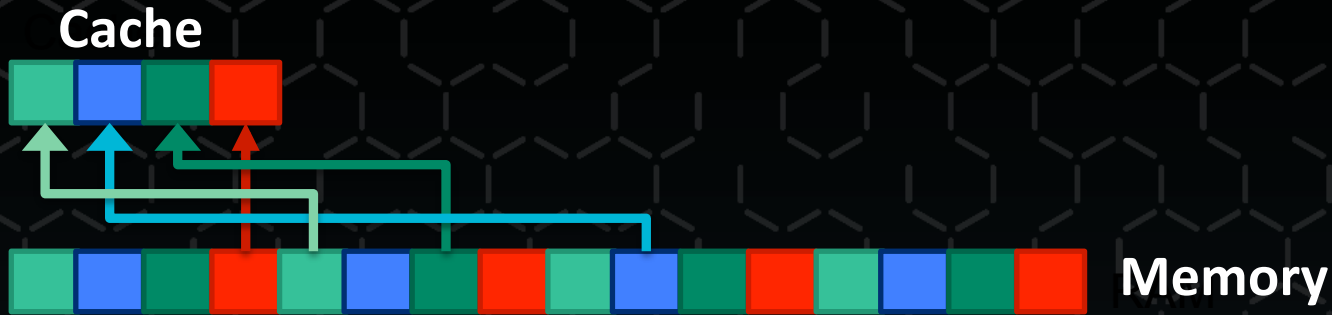
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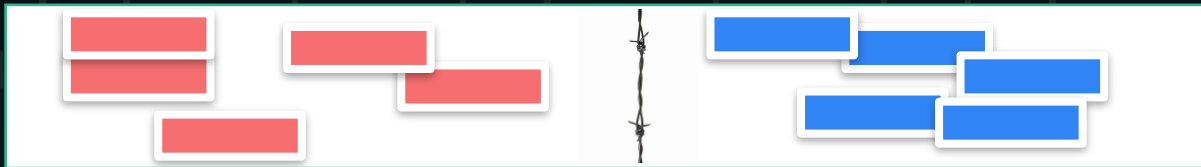
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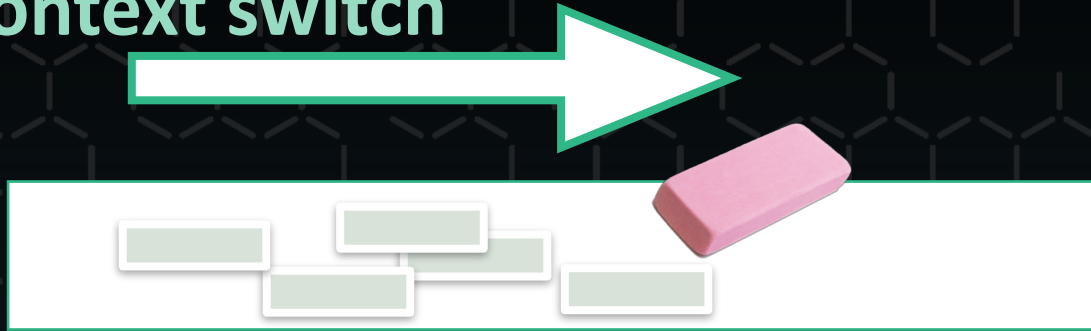
Shared hardware caches

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 - concurrent access

Cannot be supported by on-core caches

Temporal Partitioning

Context switch



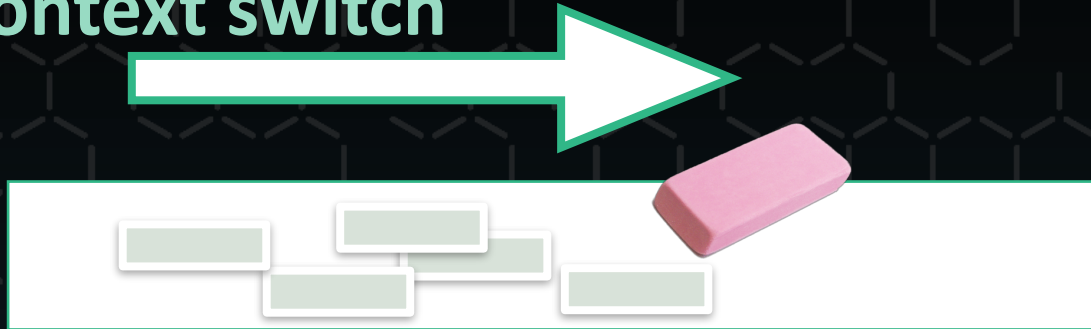
Shared on-caches

Flushing on-core caches:

- Resetting states

Temporal Partitioning

Context switch



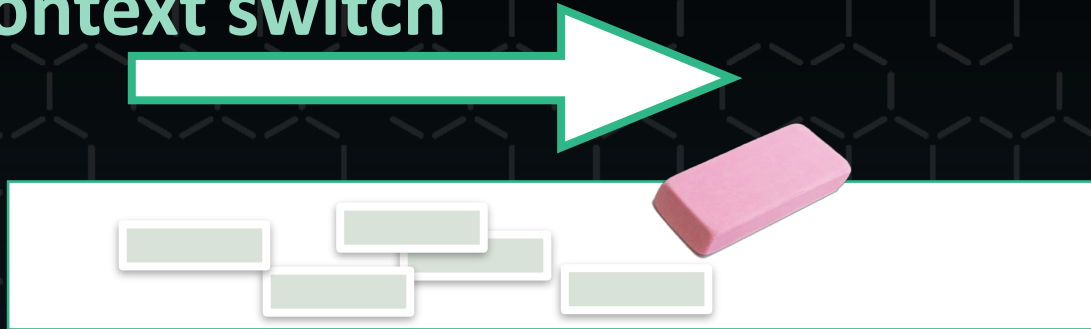
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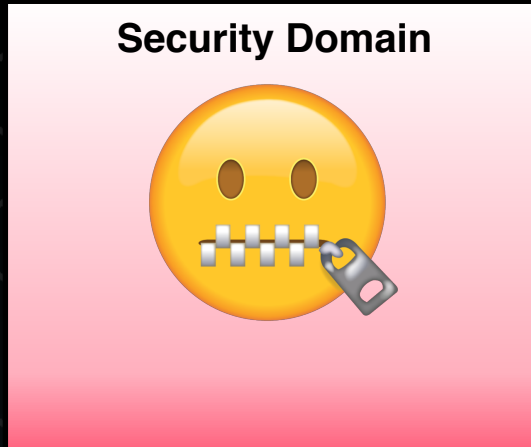
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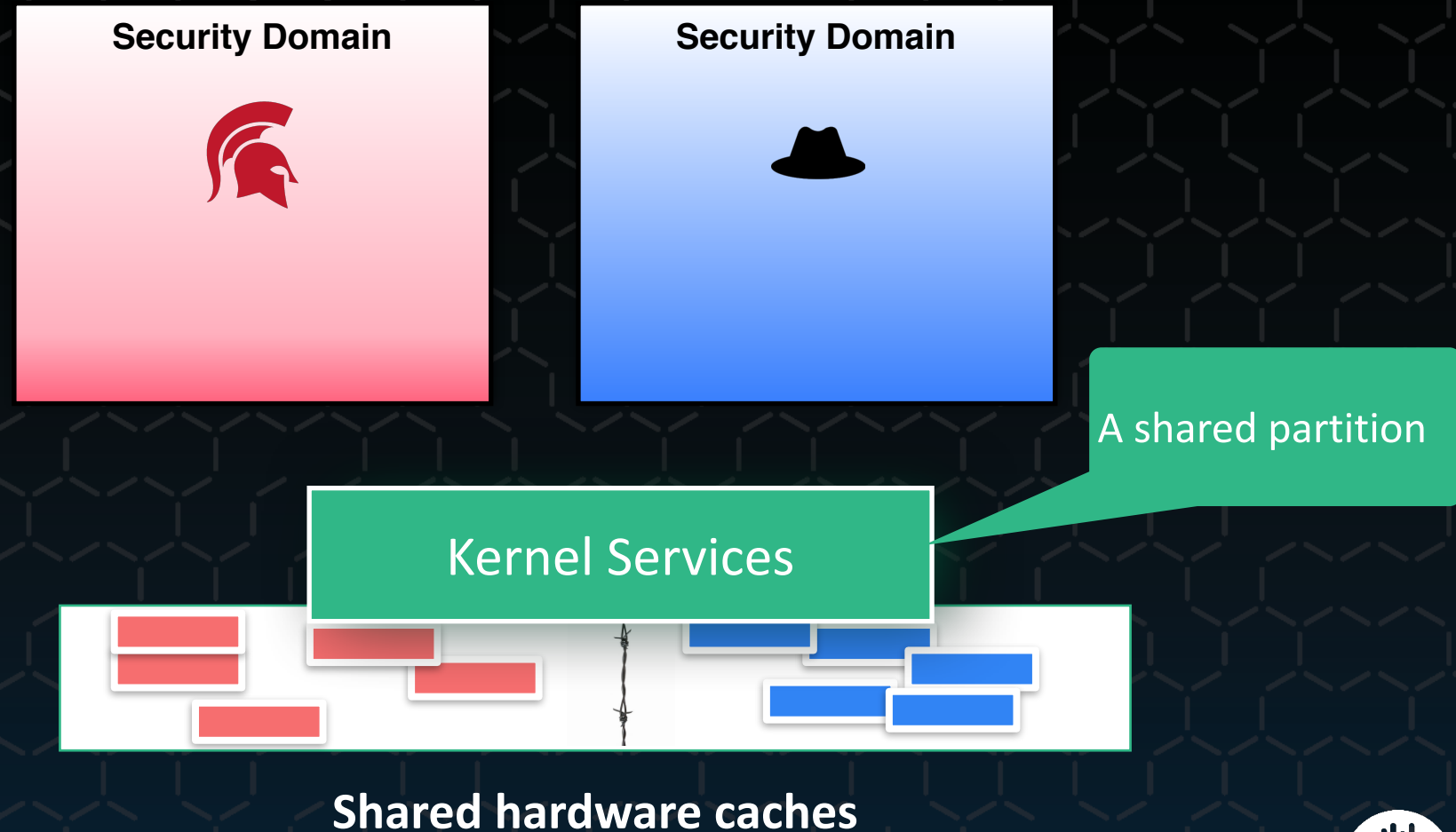
Preventing Temporal Interference through Partitioning



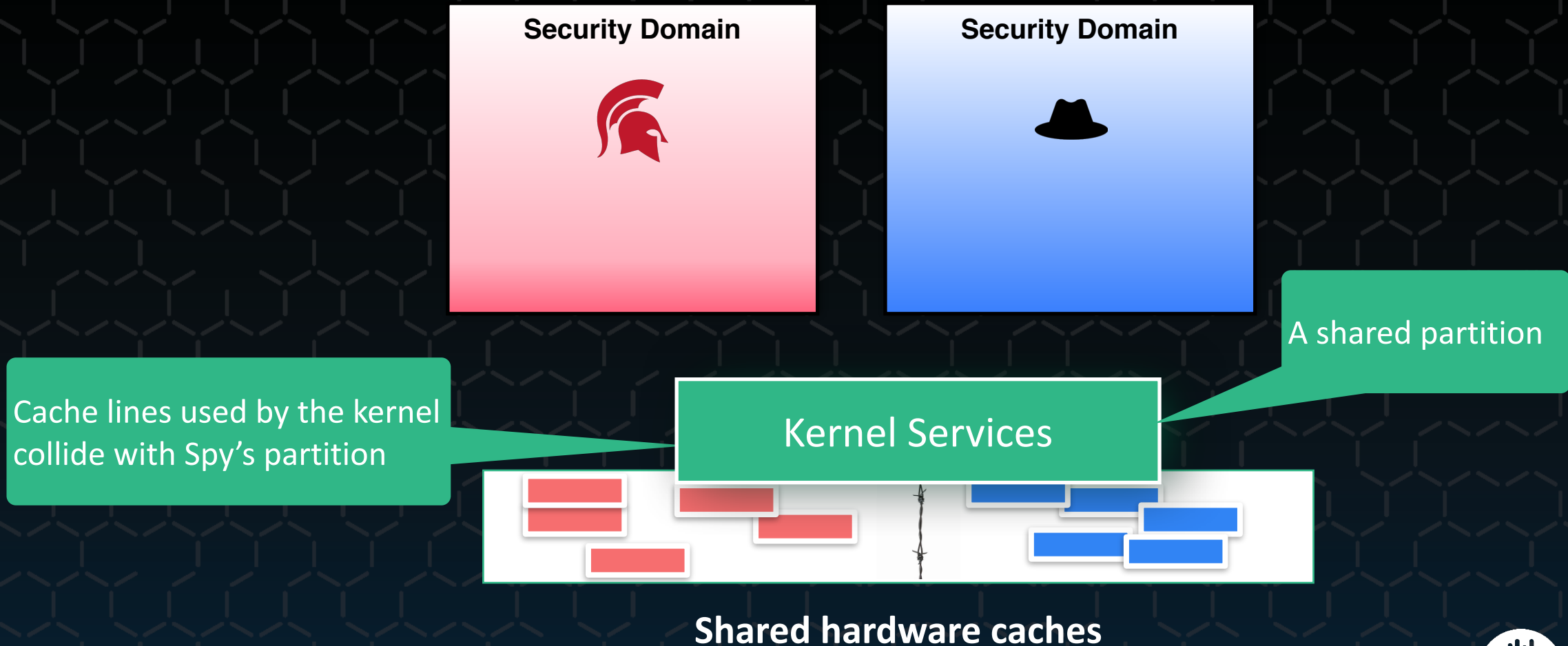
Temporal partitioning

Spatial partitioning

Wait, Everyone Shares the Kernel....

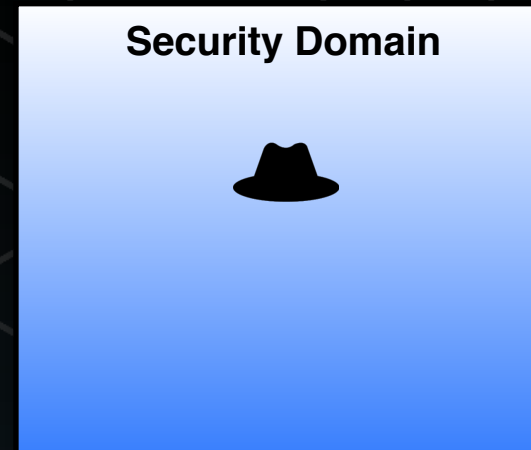
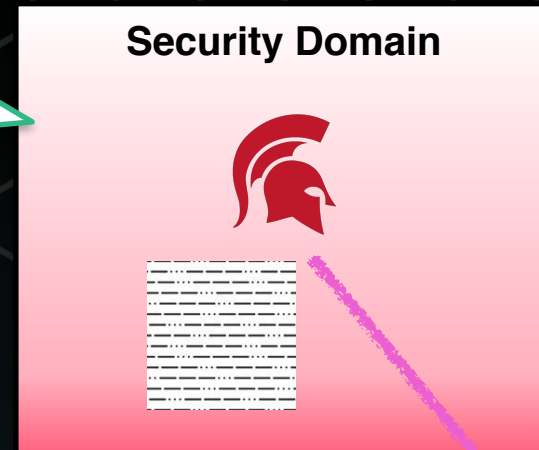


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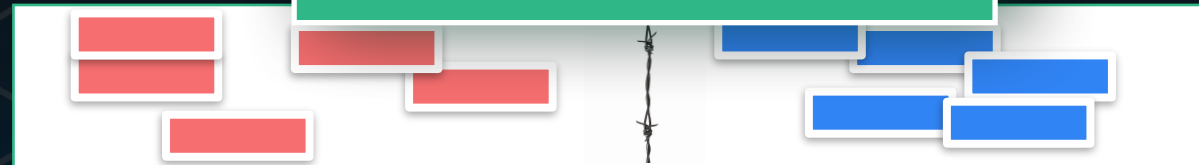
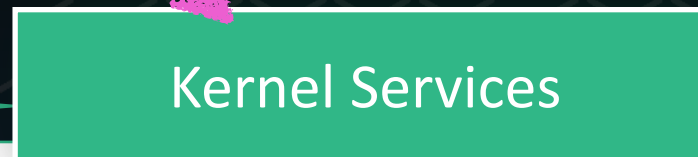
Wait, Everyone Shares the Kernel....

Poster Session
@ 17:15



Cache lines used by the kernel
collide with Spy's partition

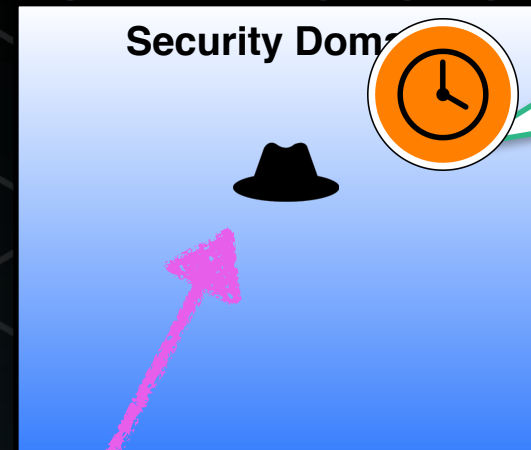
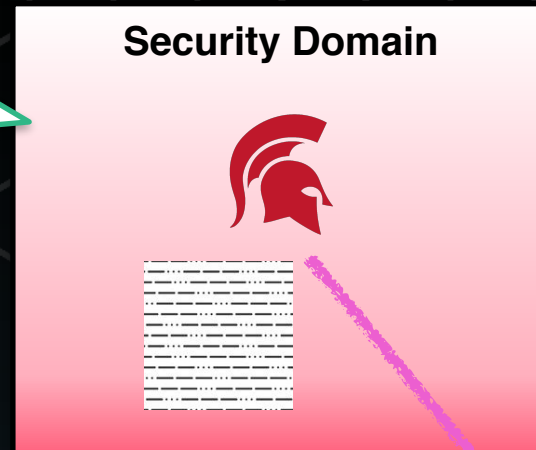
A shared partition



Shared hardware caches

Wait, Everyone Shares the Kernel....

Poster Session
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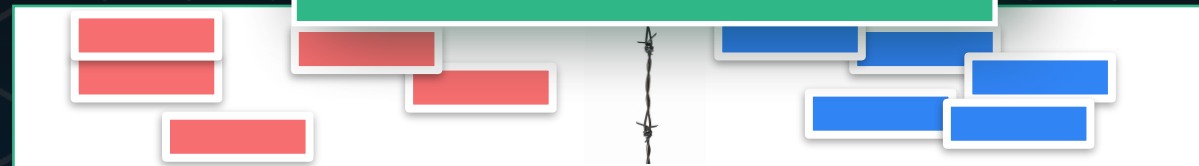


Fast Fast Slow Fast Fast
..... S F S FFF SSSS F

Cache lines used by the kernel
collide with Spy's partition

Kernel Services

A shared partition



Shared hardware caches



Kernel Services

Cloning the Kernel Image



.text

.rodata

.data

Analysing the
kernel sections

Cloning the Kernel Image



.text

.rodata

.data

Analysing the
kernel sections



.text

.rodata

.data

Global (9KiB)

Duplicated
sections

Maintaining
coherency

Cloning the Kernel Image



.text

.rodata

.data

Analysing the
kernel sections



.text

.rodata

.data

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Kernel Clone:
Generating a copy of the kernel image
with user-level managed memory

Cloning the Kernel Image



.text

.rodata

.data

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.text

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.data

Global (9KiB)

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sections

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Kernel Clone:
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Dedicated Kernel Images



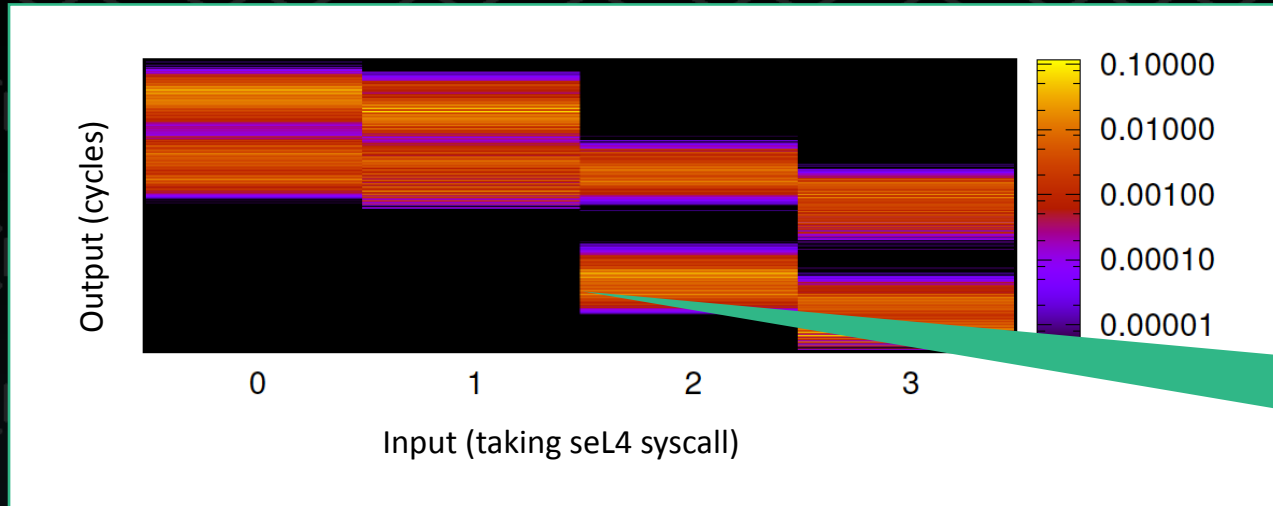
Shared Global Data

Temporal partitioning

Deterministic usage

Spatial partitioning

Timing Channel through the Shared Kernel

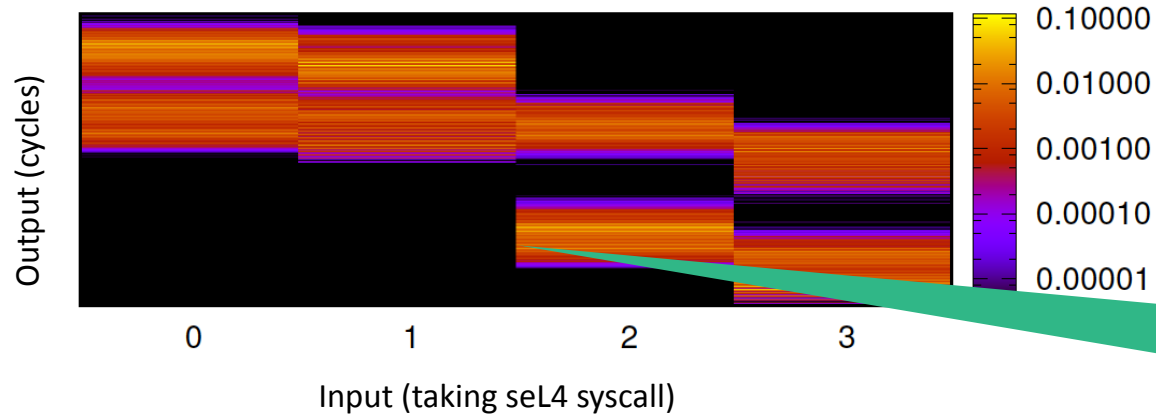


Channel matrix: conditional probability of observing the output signal (time, spy) given the input signal (system-call number, Trojan)

Raw channel

Horizontal variation indicates a channel

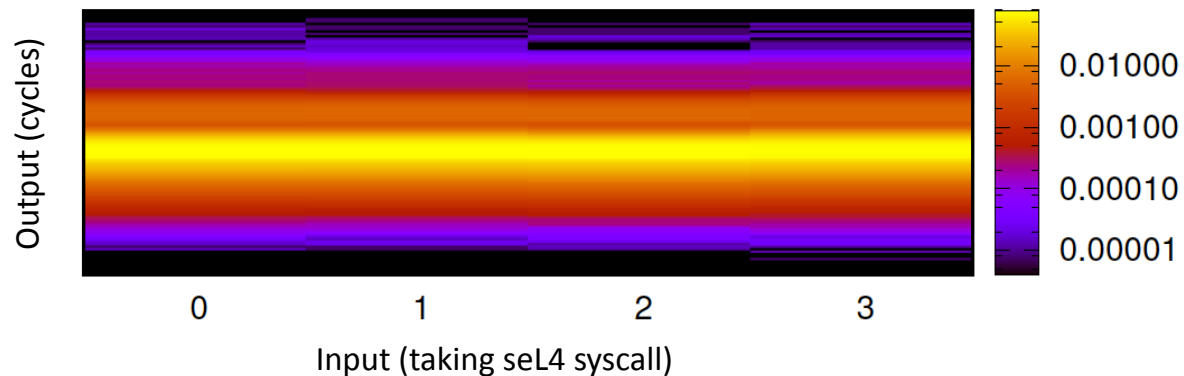
Timing Channel through the Shared Kernel



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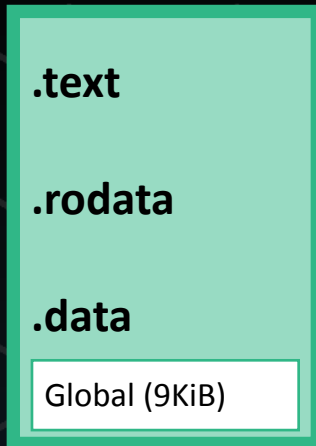
Raw channel

Horizontal variation indicates a channel



Prevented by cloned kernel

How realistic is cloning?



x86	Arm
224 KiB	120 KiB

Memory consumption

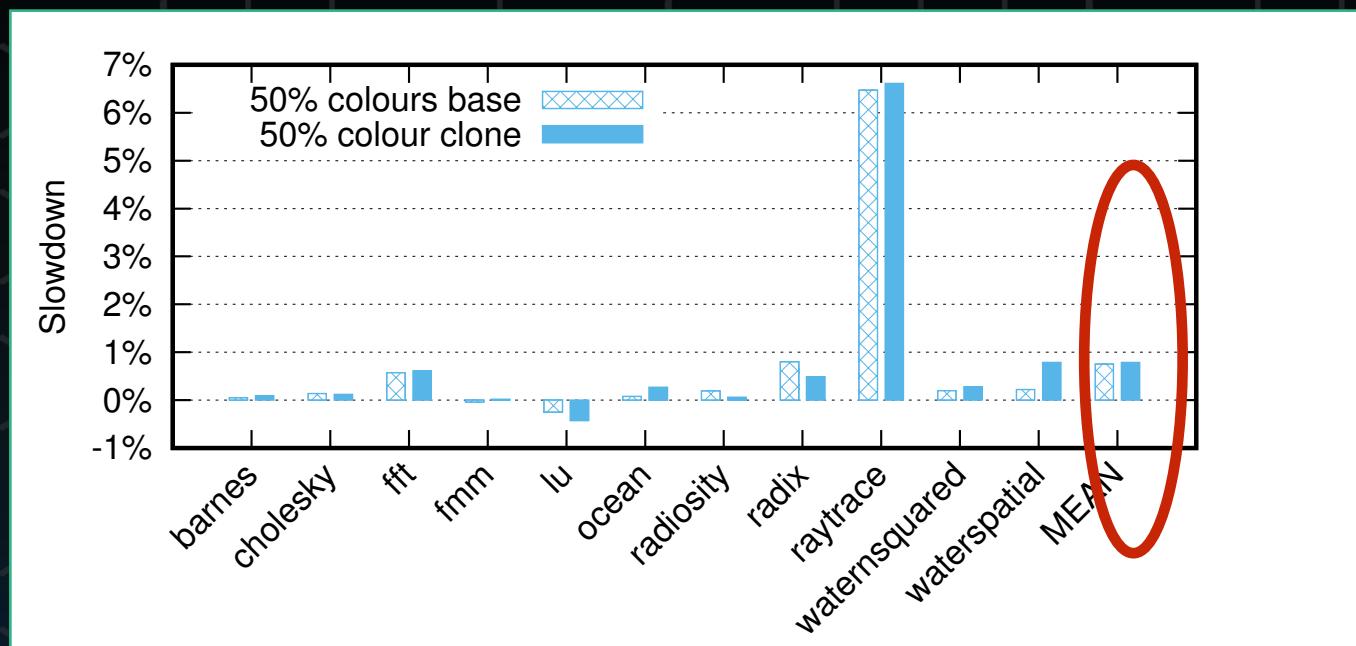
Arch	seL4 Clone	Linux fork + exec
x86	79 μ s	257 μ s
Arm	608 μ s	4,300 μ s

Efficiency

Performance Impact

The cost of colouring a domain:

- 50% of the cache colour
- 50% of the cache colour + a coloured kernel



The slowdown of splash-2 against base line kernel

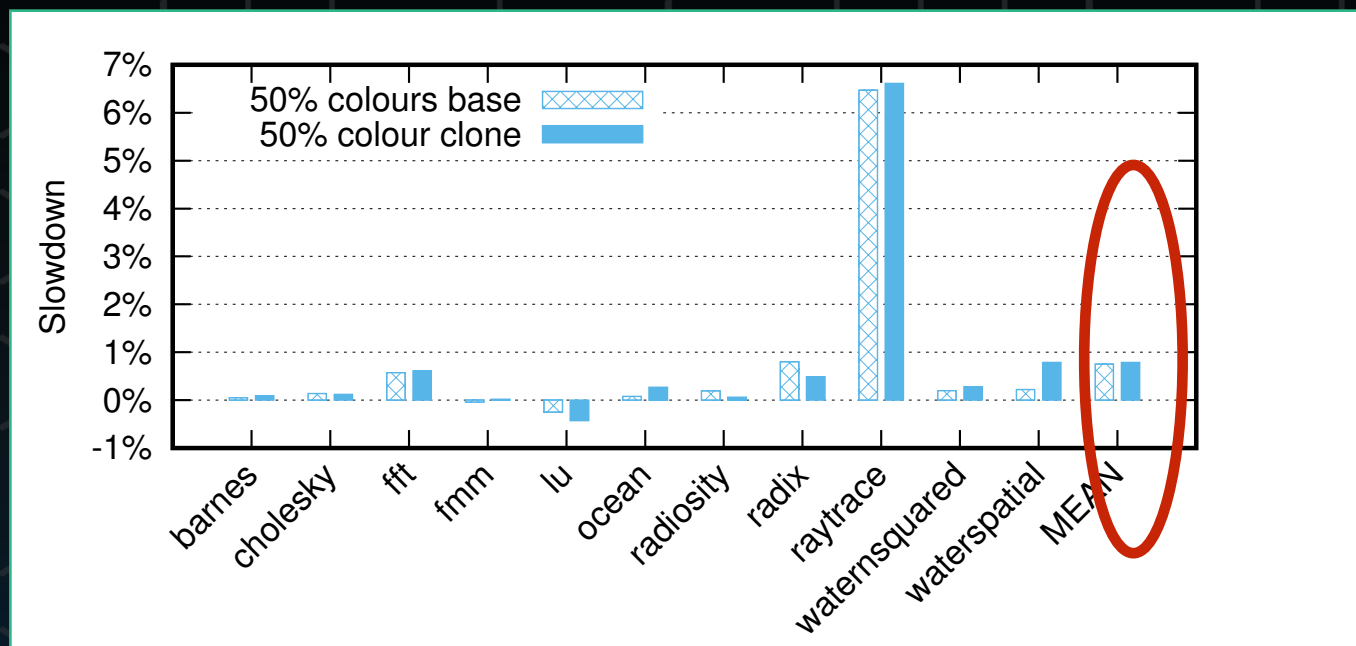
Performance Impact

The cost of colouring a domain:

- 50% of the cache colour
- 50% of the cache colour + a coloured kernel

The cost of time protection:

- spatial partition + temporal partition



x86	Arm
3.38%	1.09%

The geometric mean

The slowdown of splash-2 against base line kernel

We have also done:

- Partition IRQs
- Domain-switch actions
- A deterministic domain switching latency
- Preventing timing channels:
 - Shared kernel, Intra-core, cross-core, domain-switch latency, timer
- Performance evaluation:
 - IPC, domain switching latency, kernel cloning, cache colouring, time protection

Summary

- Define temporal isolation as a mandatory (black-box mechanisms) enforcement provided by the OS.
- Time protection for preventing microarchitectural timing channels
- Effective on closing studied timing channels
- Low overhead





THANK YOU

Trustworthy Systems

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w <https://ts.data61.csiro.au/projects/TS/timingchannels/>

www.data61.csiro.au

