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Operating System Support for the Heterogeneous OMAP4430:

A tale of two micros

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with Aaron Carroll and Bernard Blackham

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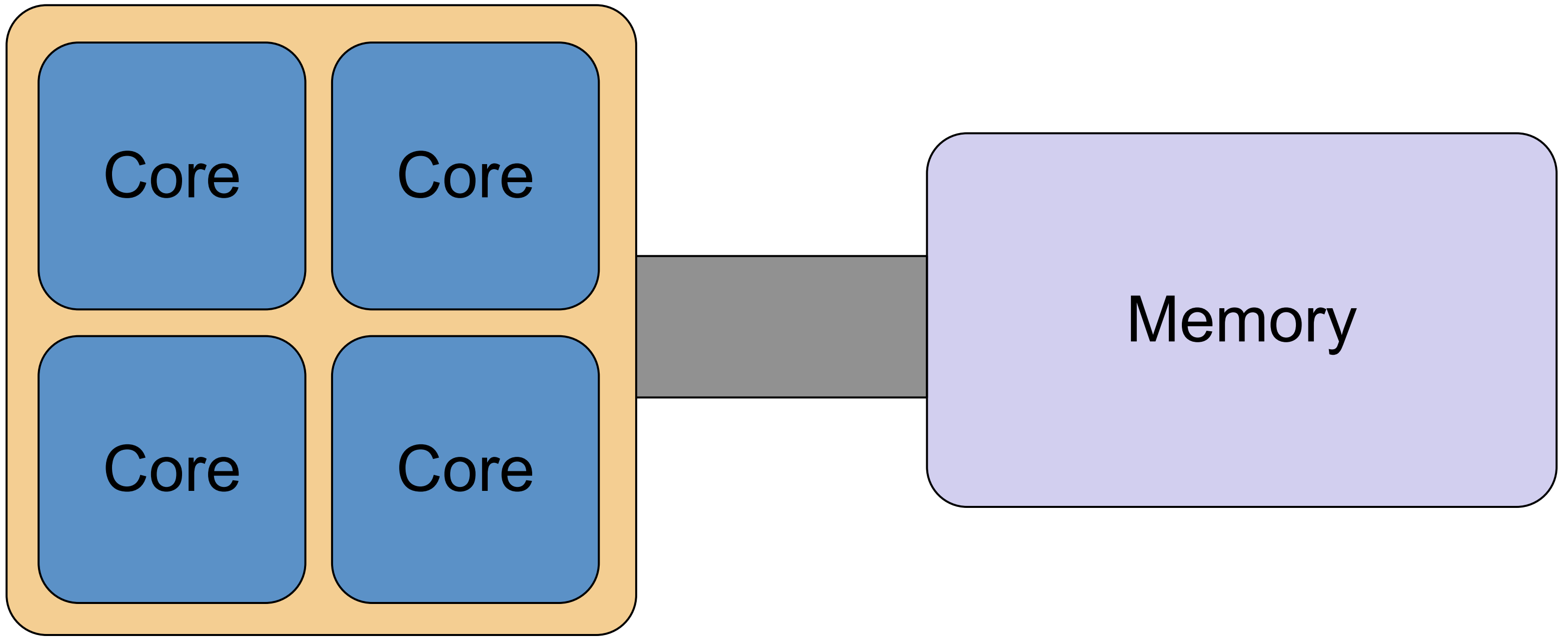
Traditional chip-multi-processors

- Symmetric Multi-Processing (SMP)
  - – two or more identical processors / cores



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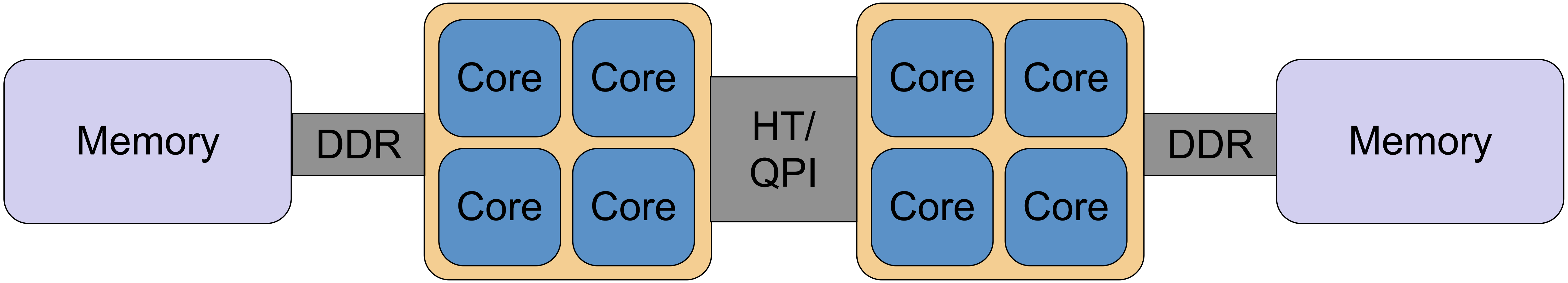
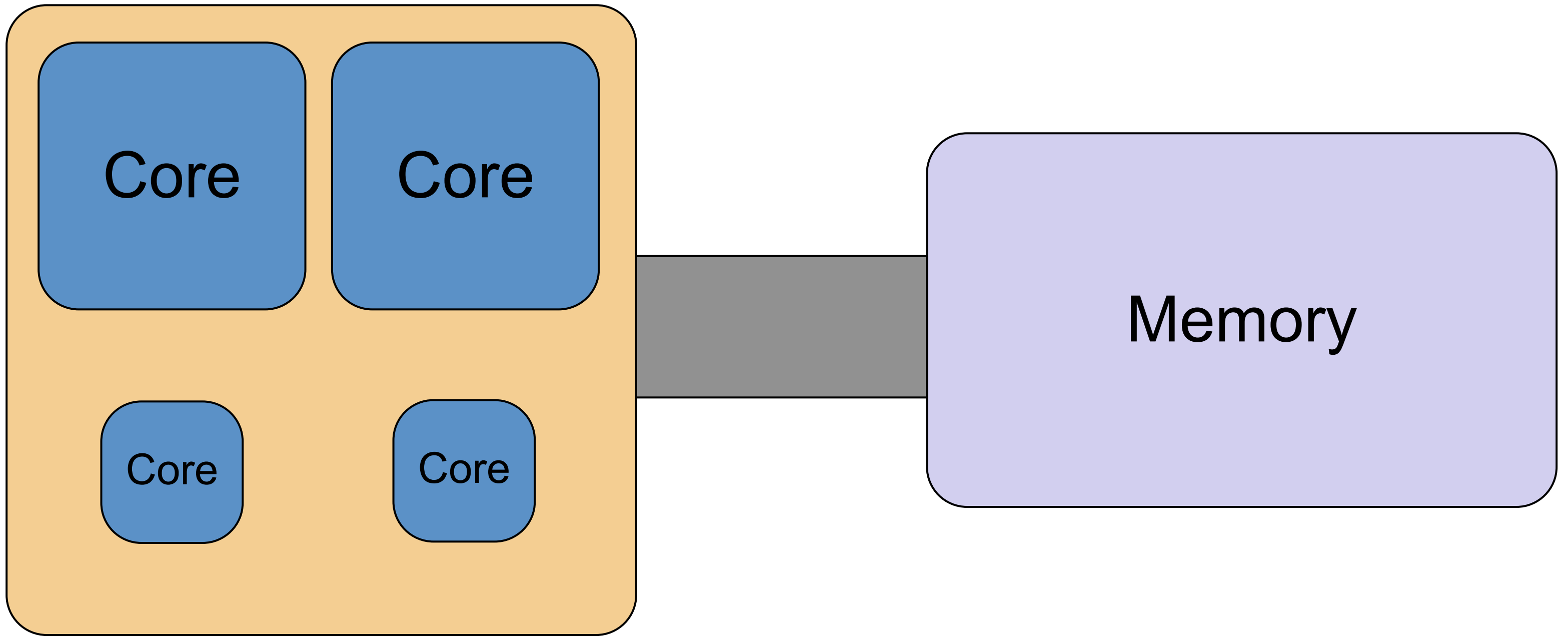
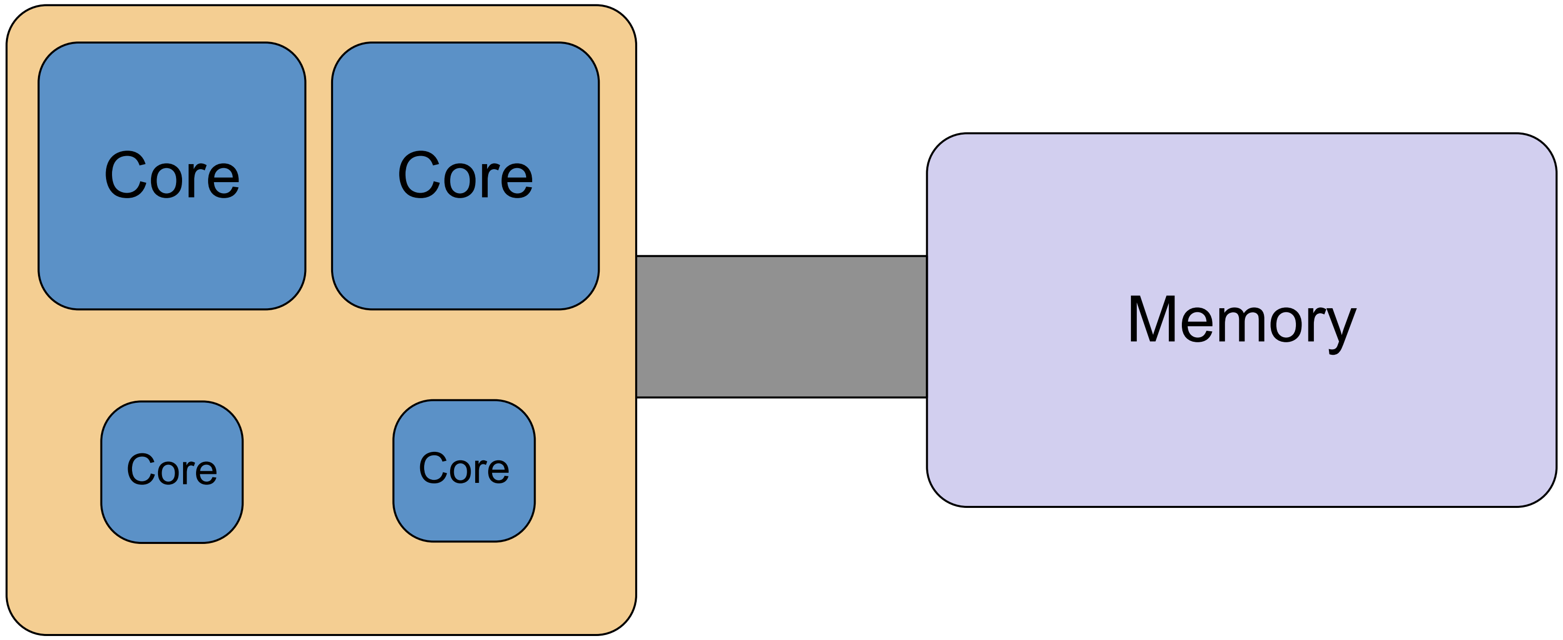


Heterogeneous chip-multi-processors

- ‘Asymmetric Multi-Processing’ (AMP)
  - – several different processors / cores



Core asymmetry



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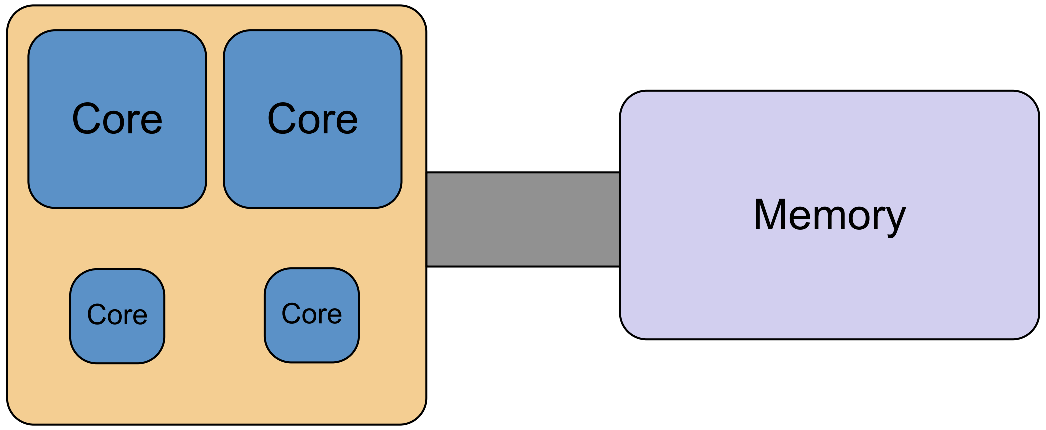
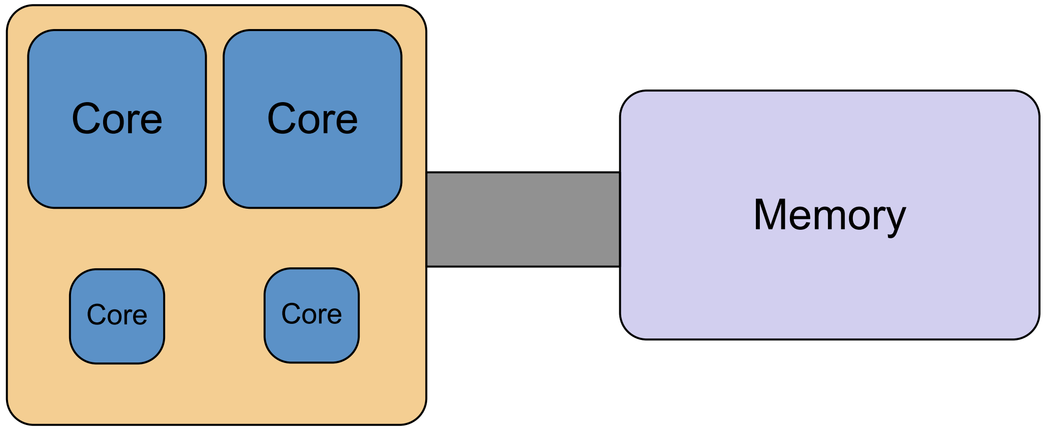


Core asymmetry

- Performance
  - – different frequency
  - – different pipelines
  - – different size caches/TLBs
  - – etc.



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  - different pipelines
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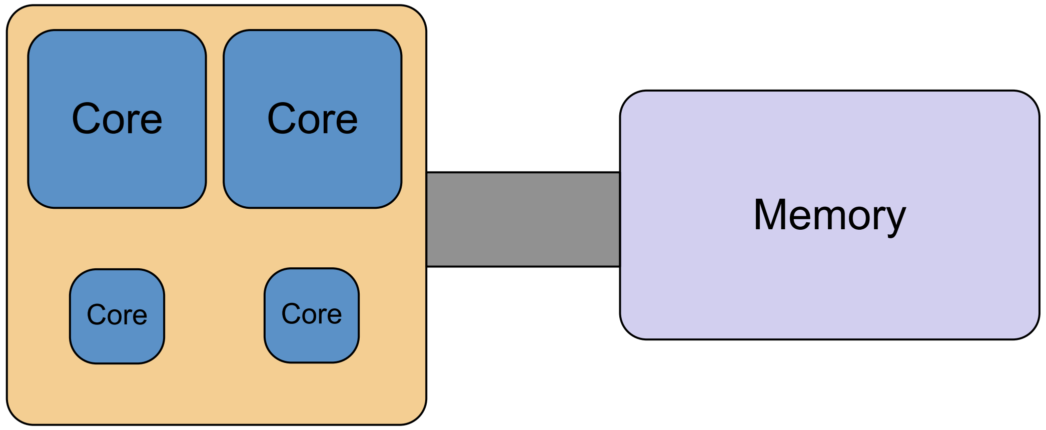
  - etc.
- Instruction Set Architecture
  - ARMv7 vs Thumb
  - SSE vs no SSE



Benefits of heterogeneous systems

- Energy efficiency
  - small cores have a small die area
  - low-power off-load allows big cores to sleep while small cores work
- Computational efficiency in general
  - can fit more small cores in a given area giving greater parallel performance
  - single-threaded workloads can still get performance on a big core

OS design for heterogeneous processors

- Models
  - restrictive
  - hybrid
  - unified
  - distributed

Restrictive model

- Restrict all programs to the sub set of features supported by both types of cores
- Limited to a subset of features
  - performance may not be as good as it could be

Hybrid model

- Allow user programs to interrogate the heterogenous capabilities of the system
- Allows user programs to execute on the cores that provide the features they need.
  - on Intel, CPUID
  - sched_setaffinity(target_core)

Unified model

- Allow programs to use the combined feature set of the two types of cores
- Fault-and-migrate when an unsupported feature is requested
- *Proxy* instructions in light-weight processes
- Requires a lot of OS trickery

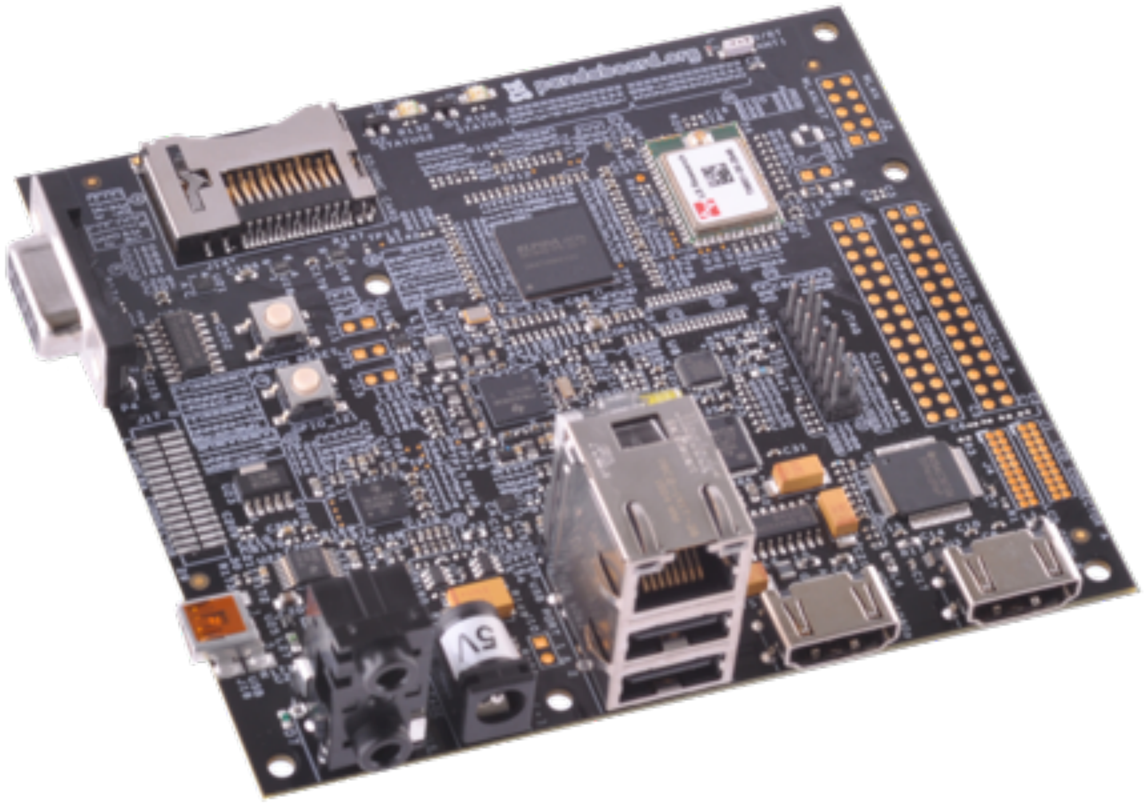
Distributed shared-memory model

Distributed shared-memory model

- Simply provide a mechanism for loading and running code on different cores
  - SPUfs
    - IBM Cell processor
    - filesystem based, at least it fits the Unix model!
  - TI SysLink
    - provides mechanism to load software into co-processors
    - runs within the TI SYS/BIOS OS framework

Pandaboard

- USB, DVI/HDMI, Ethernet, WiFi, Bluetooth, SD-card, etc…



The first OMAP4430 hardware platform

PEAP project

- TI gave us a free Pandaboard!
  - *Pandaboard Early Adopter Program* (PEAP)
  - project chosen from about 50 potentials
- The plan was...
  - a single Linux image running on both architectures
  - treat both types of core as general-purpose
  - examine effects on
    - Energy consumption
    - Efficiency

TI OMAP 4430

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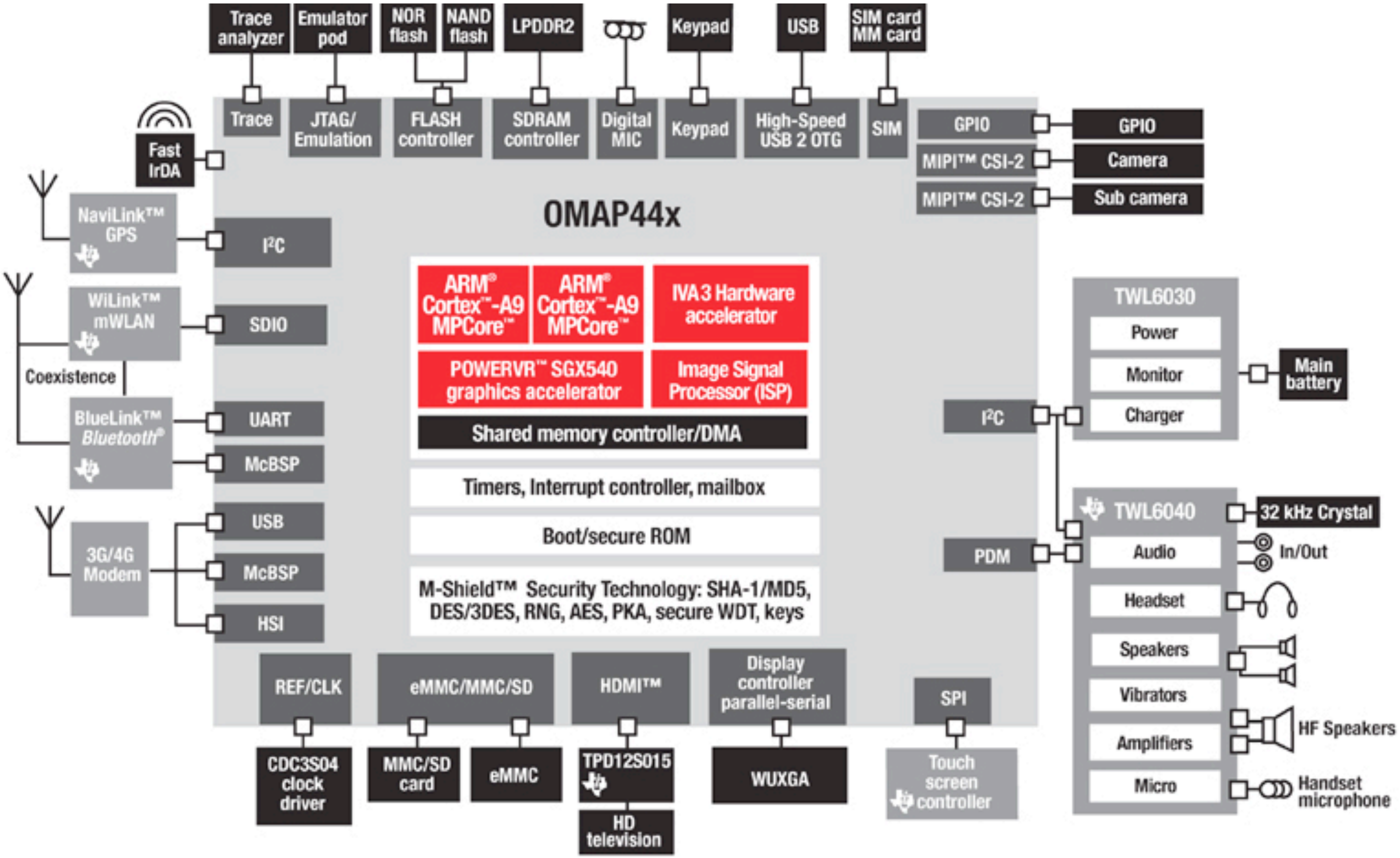
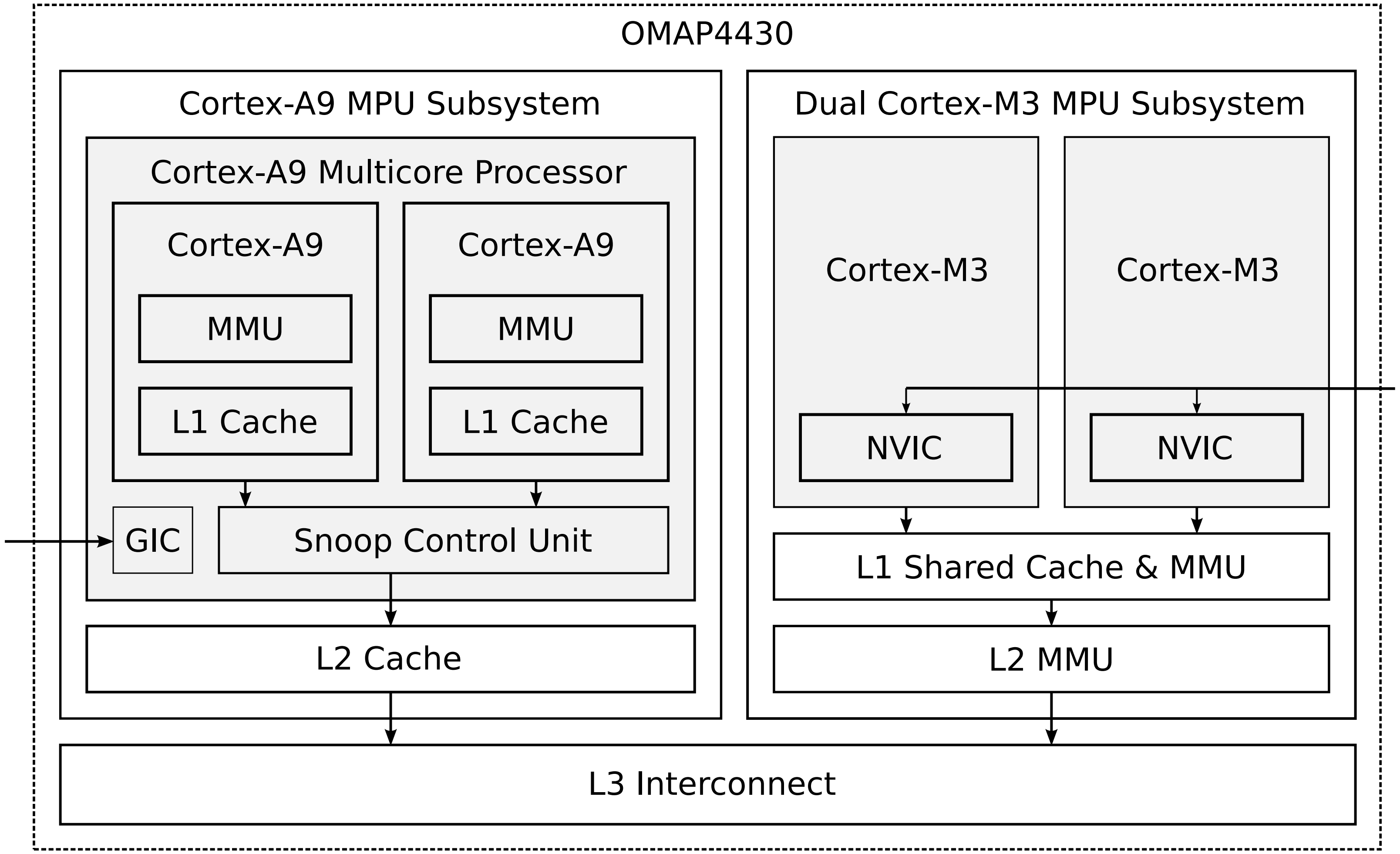


What cores?



	ARM Cortex-A9 Core	ARM Cortex-M3 Core
Architecture	ARM v7-A	ARM v7-M
ISA Support	ARM, Thumb-2, floating-point, NEON, DSP, Jazelle	Thumb-2
Memory Protection	Memory Management Unit	Optional 8 region MPU
Clock Speed	1.0 GHz	266 MHz

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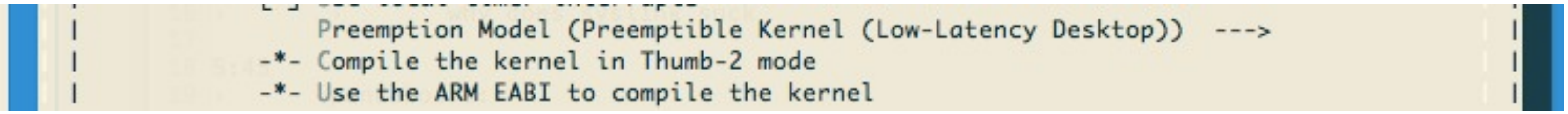
- System ISA is also completely different

Thumb-2 support for kernel



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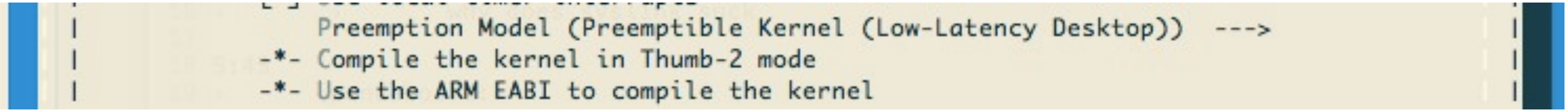

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  - – a small amount of assembly hacking
  - – found bug in OMAP init routines, booting second core in ARM mode
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    - ABI defines them as ARM
    - glibc tries to put the CPU in ARM mode
    - patch glibc! more later...

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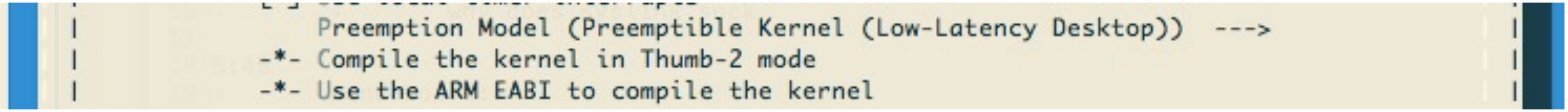

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- It works!

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A second step...

...Linux on the Cortex-M3!

- Standard Linux does not support the Cortex-M3 **:-(**
  - M3 core is designed for small embedded systems without a MMU
- uClinux support exists
  - fork of Linux designed to support small micro-controllers
- Our plan
  - take the support from uClinux and put it into standard Linux
  - Linux can't directly boot an M3 core, so...
  - partition memory in two
  - bootstrap M3 Linux from A9 Linux

Problems with Linux on the Cortex-M3

- Memory management
- Exception handling
- Toolchain

Memory management

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- Page table
  - – virtual-to-physical memory mappings

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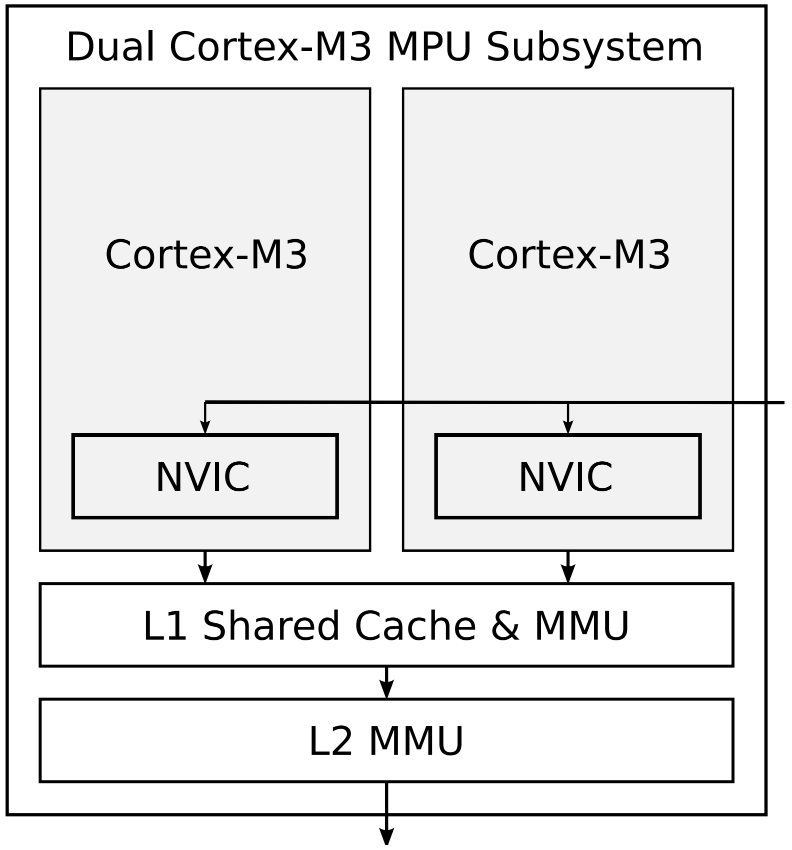
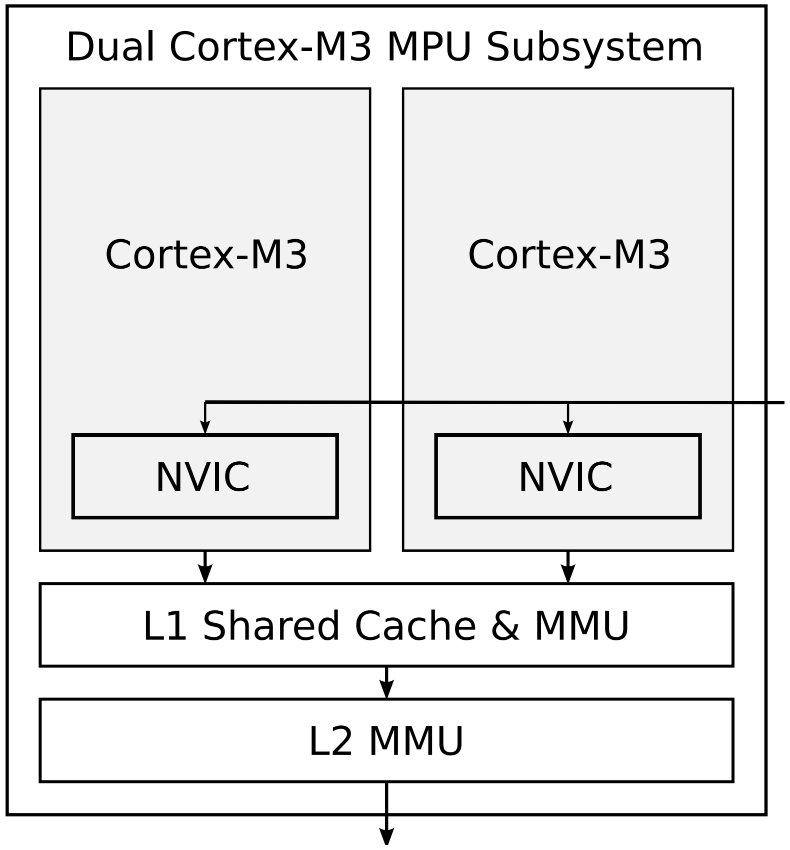
- Translation look-aside buffer (TLB)
  - cache for virtual memory mappings
  - software loaded
  - hardware pagetable walker

Memory management on the Cortex-M3



Memory management on the Cortex-M3

- Subsystem's shared MMUs
  - L1 shared cache & MMU
    - 10 entry TLB
    - read-only & execute-only permissions
    - software loaded
  - L2 MMU
    - 32 entry TLB
    - hardware walker (ARMv6 without permissions)



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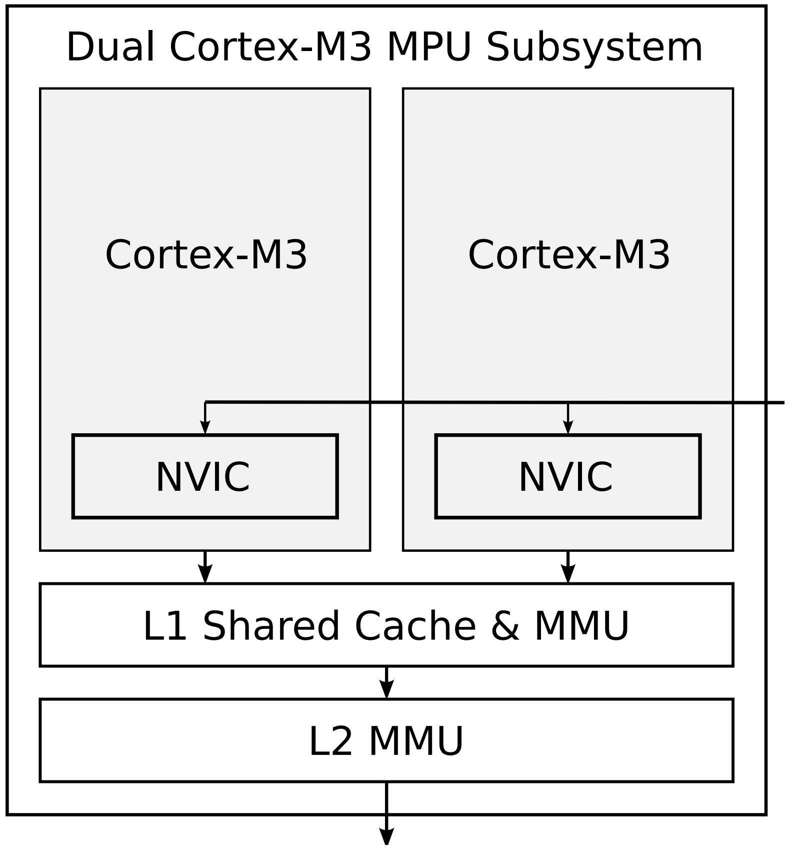

- Limitations
  - no supervisor-mode permissions - separate kernel page table
  - no tagged TLB - flush the TLB on every context switch

Copy on write

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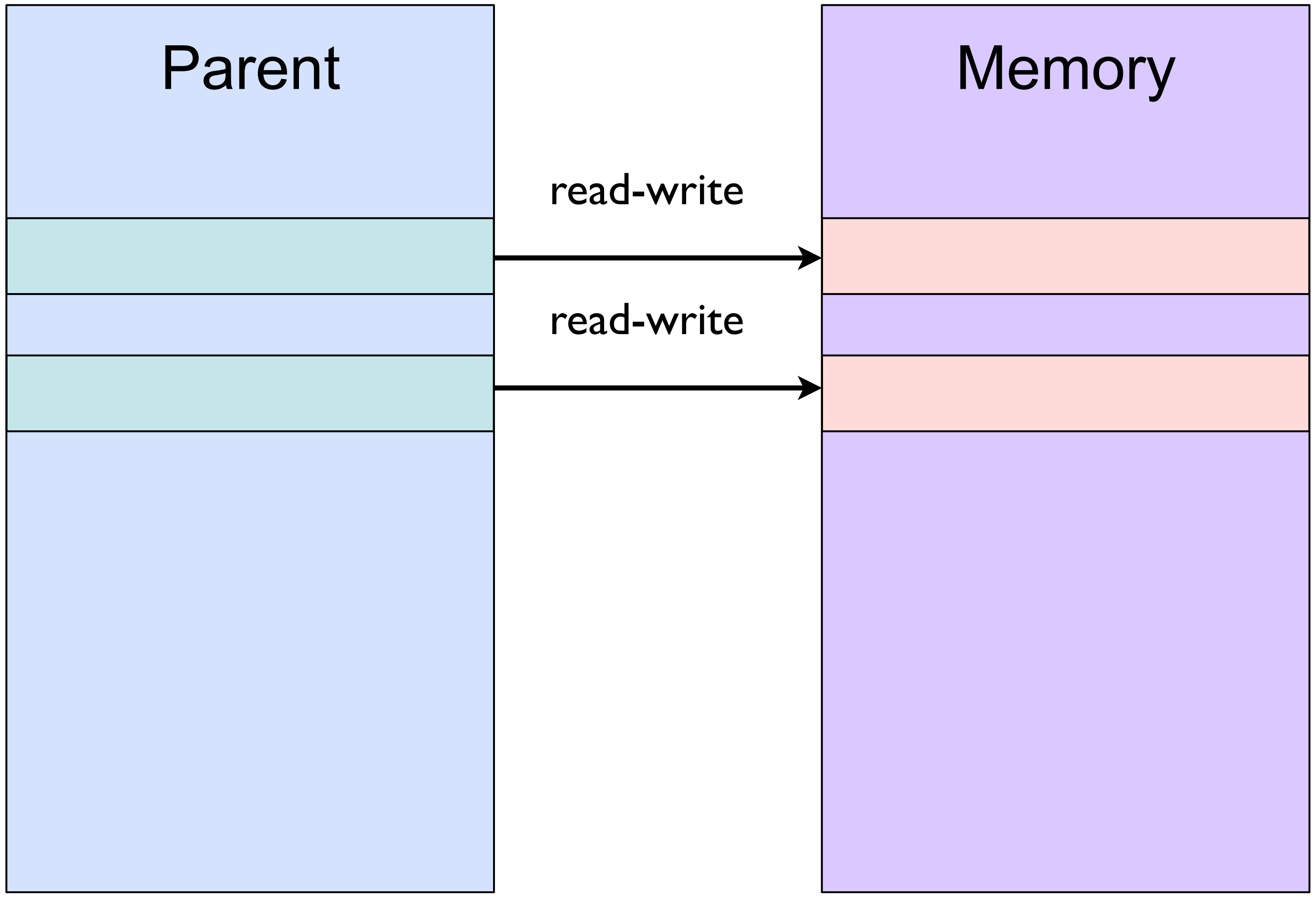

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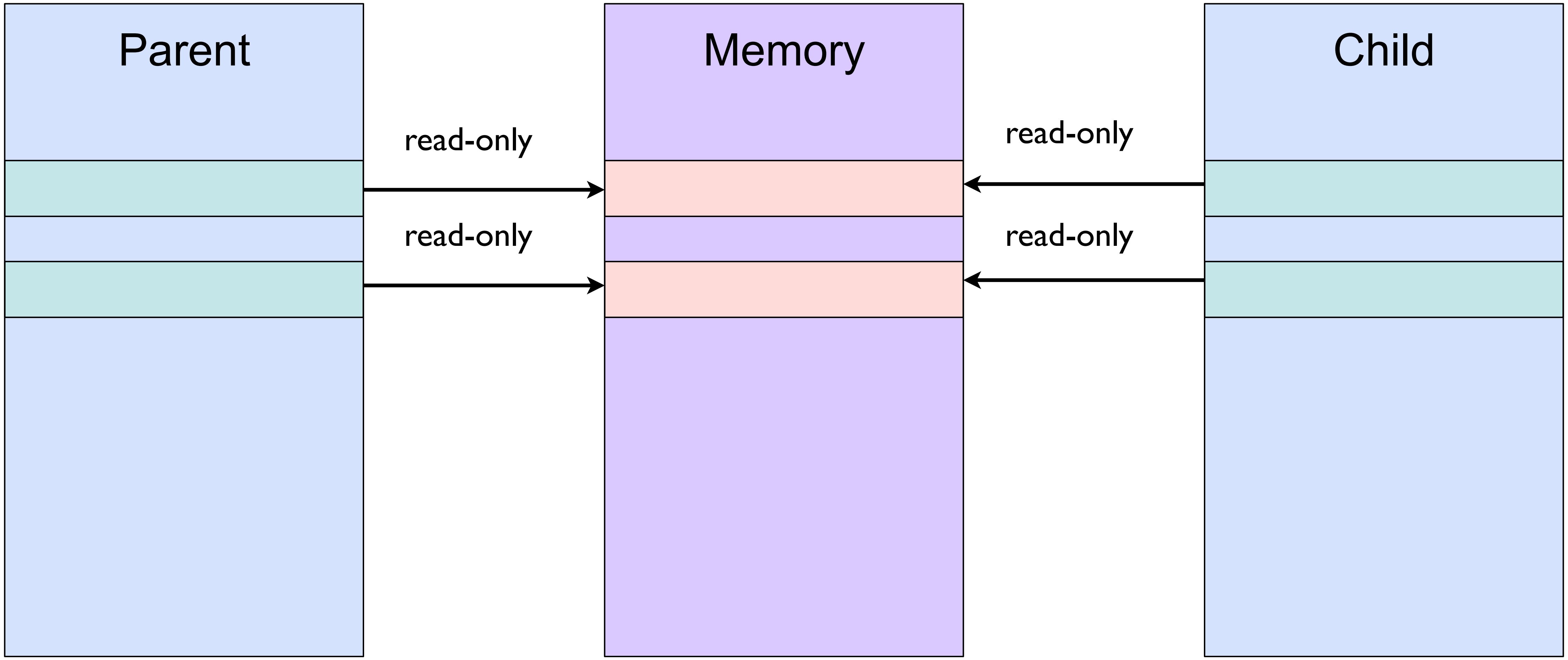

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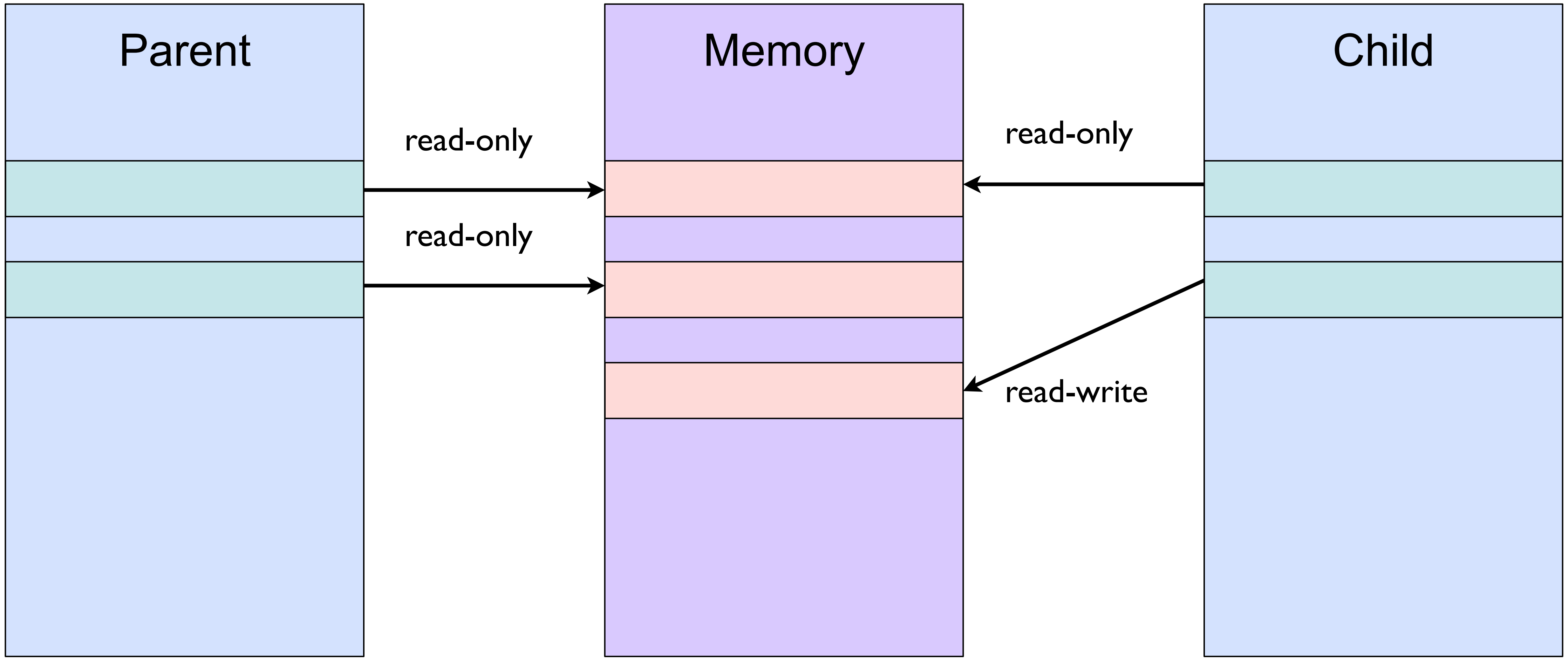

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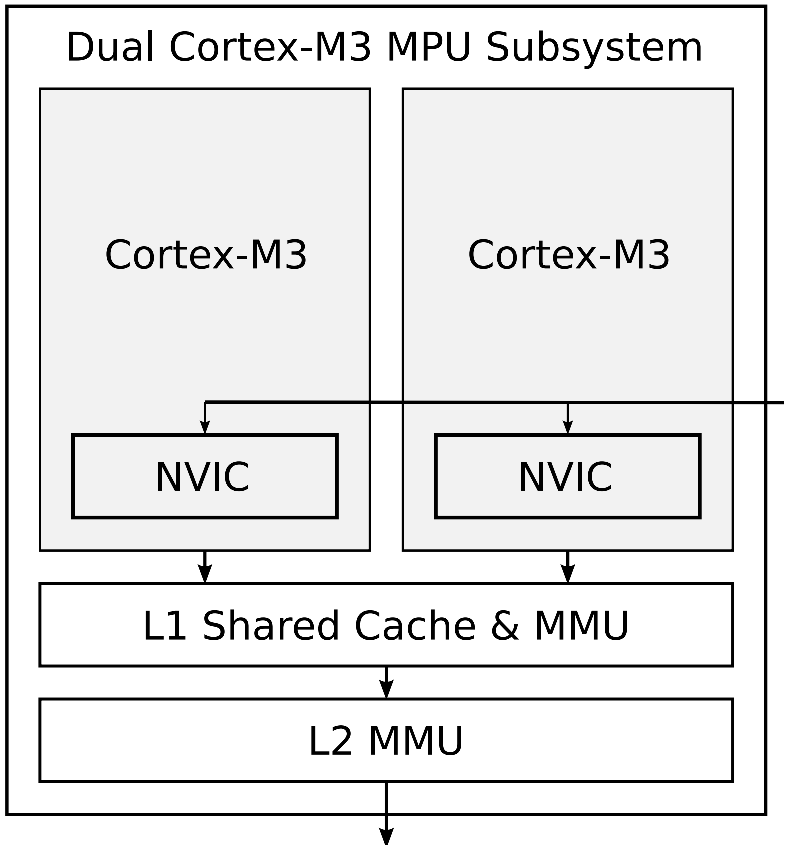

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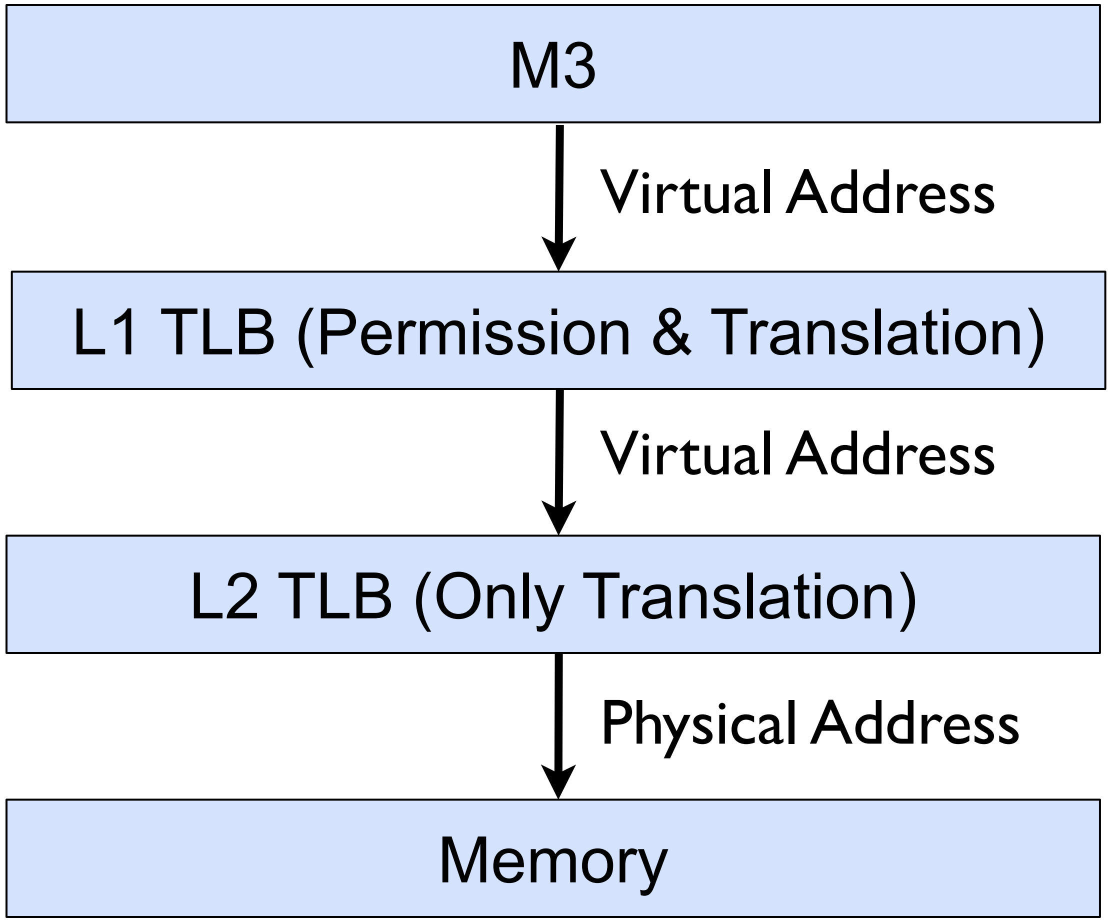
Read-only pages

- Hidden from L2 walker
  - marked invalid in the pagetable
  - causes a fault when access
- Manually loaded into L1
  - with correct permissions
  - no translation
- L2 kept in sync with the L1
  - MMUs in series, double translation
  - avoid L2 faulting



M3

Virtual Address

L1 TLB (Permission & Translation)

Virtual Address

L2 TLB (Only Translation)

Physical Address

Memory

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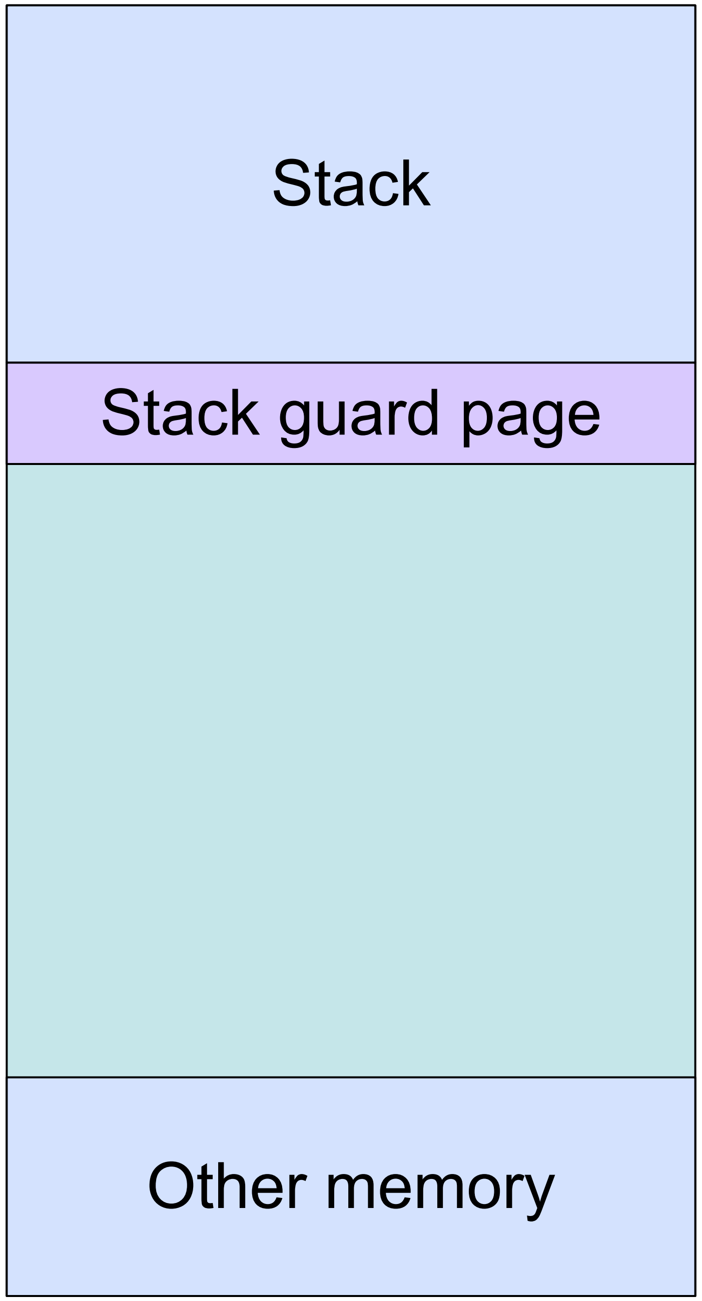

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- Dynamic stack allocation
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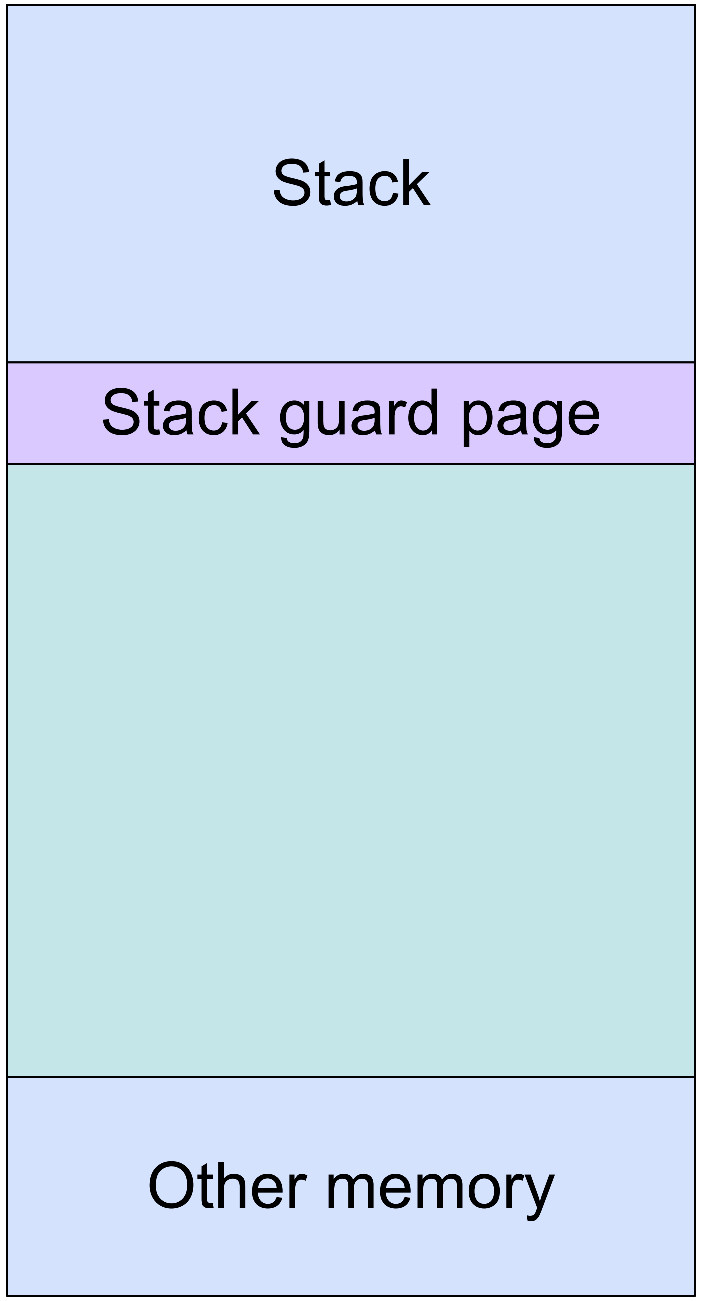
- Stack faults on M3 are unrecoverable
  - preallocate and pin entire stack
  - no dynamically resizing the stack



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  - hand coded ARM assembly, e.g. memcpy implemented in ARM assembly
- Binutils
  - Procedure Linkage Table (PLT) used for dynamic binding shared libraries implemented with ARM
  - stick with static binaries for now

Linux now works on the M3 and supports userspace...

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… beside an A9

Modifying Linux to support the A9s and M3s

- Unified model
  - performance overhead of migrations
- Hybrid model
  - no forced restriction of features
  - allow the user to interrogate system
- Restrictive model
  - restrict to subset of features
  - allows any process to run on any core

Implementing this in Linux

- Compiling for the subset of Thumb-2
- Producing a single image
- Synchronisation
- Supporting live migration
- Interrupts

Compiling for multiple architectures

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- Compile a single image which can boot either A9 or M3
- Patched binutils
  - compile C to common subset of Thumb-2
  - allow for both architecture's special register/co-processor instructions
    - cp15 (A9 co-processors for system control, cache, MMU)
    - PRIMASK, FAULTMASK, BASEPRI (M3 mask registers)

Single kernel image

Single kernel image

- ARM Linux can be compiled for multiple processors
  - multiple processor abstraction (proc_info)
    - allows compiling support for multiple processors into a single image
  - extended to incorporate architectural (system ISA) differences
    - interrupt enabling/disabling, co-processors, exception handling

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  - – extended to incorporate architectural (system ISA) differences
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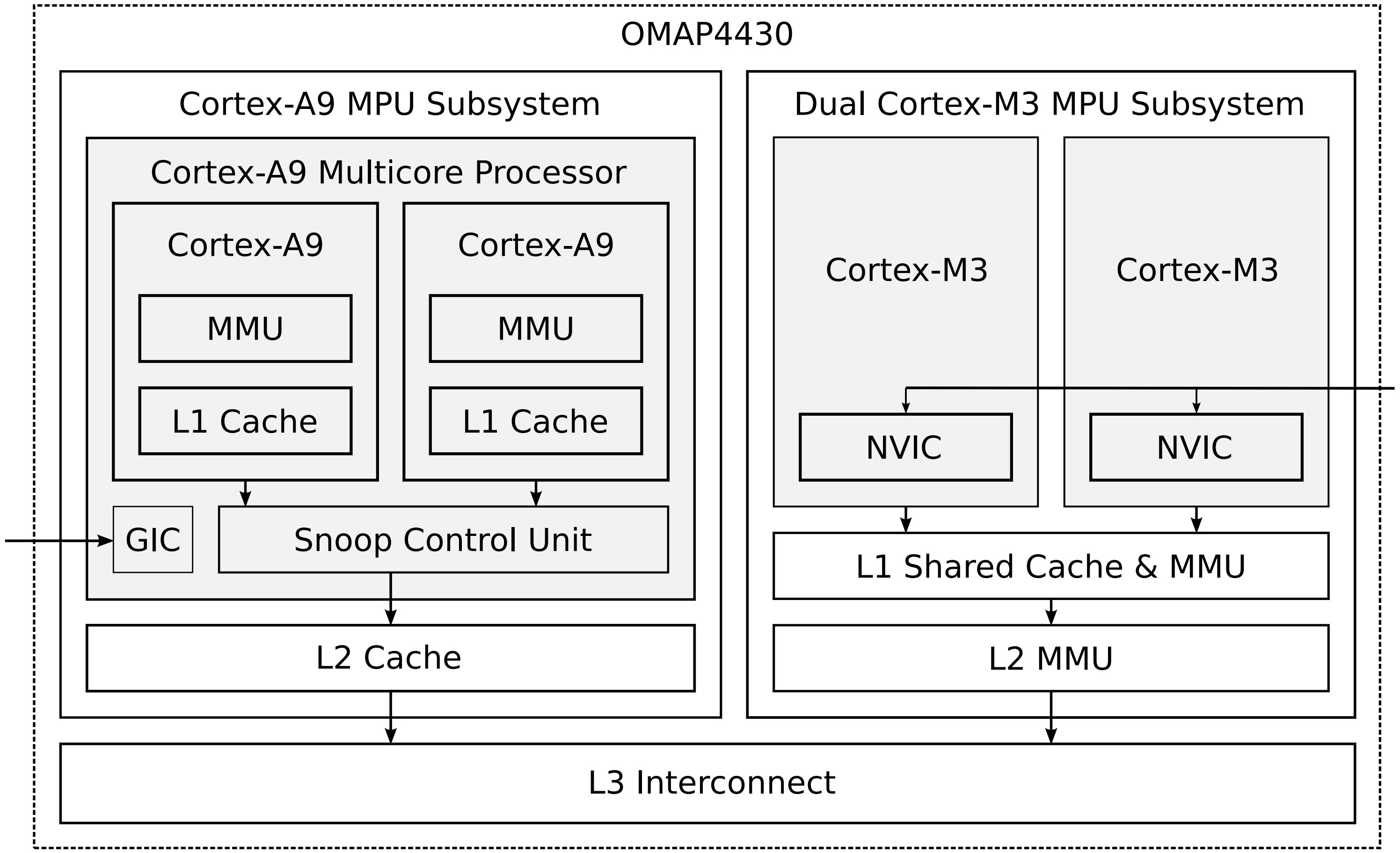
- Running the kernel on both A9 and M3
  - – per core (A9/M3) MMU mapping for proc_info struct, each core can see its own functions

Synchronisation

- Cross-subsystem synchronisation
  - locks are implemented using an atomic operation
  - ARM's *exclusive monitor* won't work (LDREX, STREX)
  - implement synchronisation primitives with hardware spin-locks



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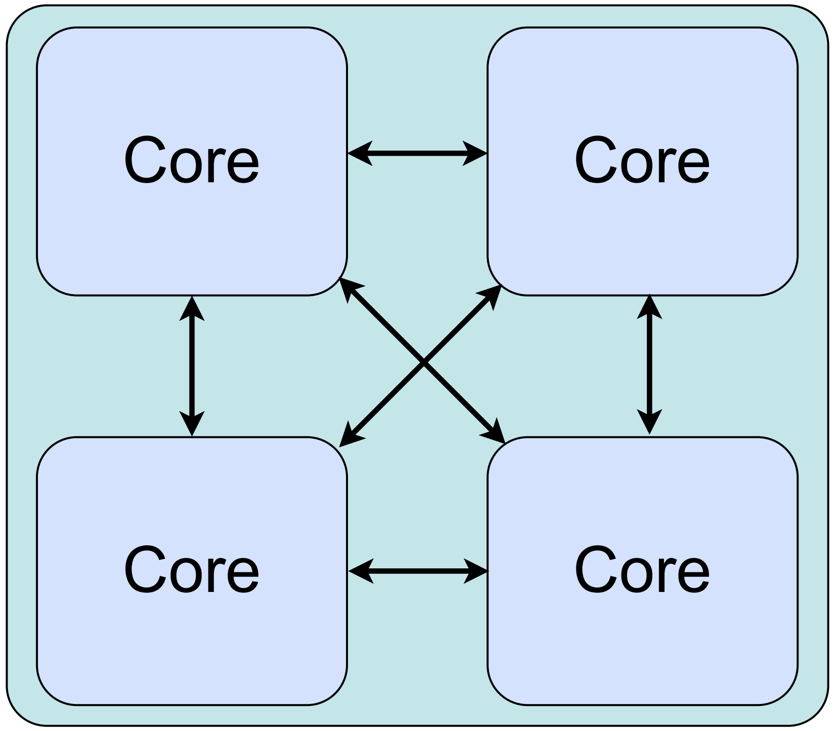

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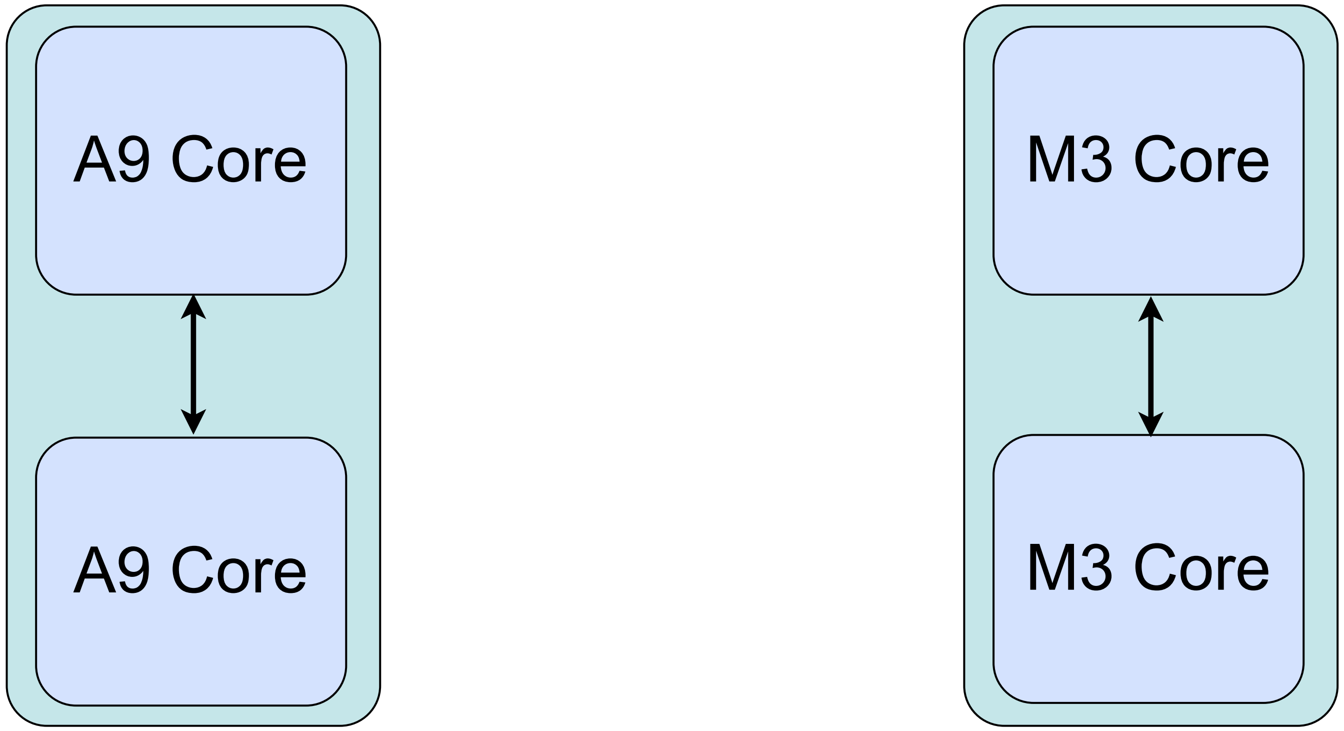

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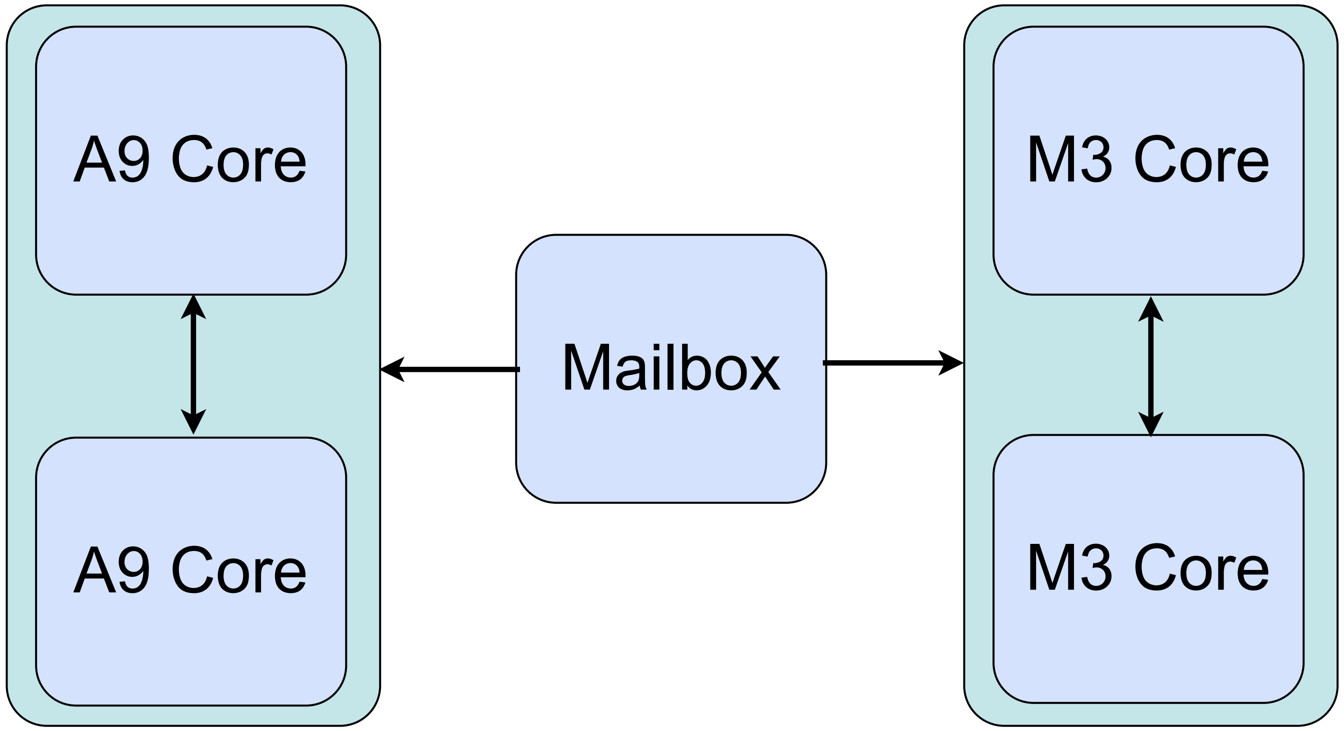

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- Exception handling
  - manipulate status registers and saved registers to consistent format
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- Live migration
  - taskset, sched_setaffinity

Interrupts

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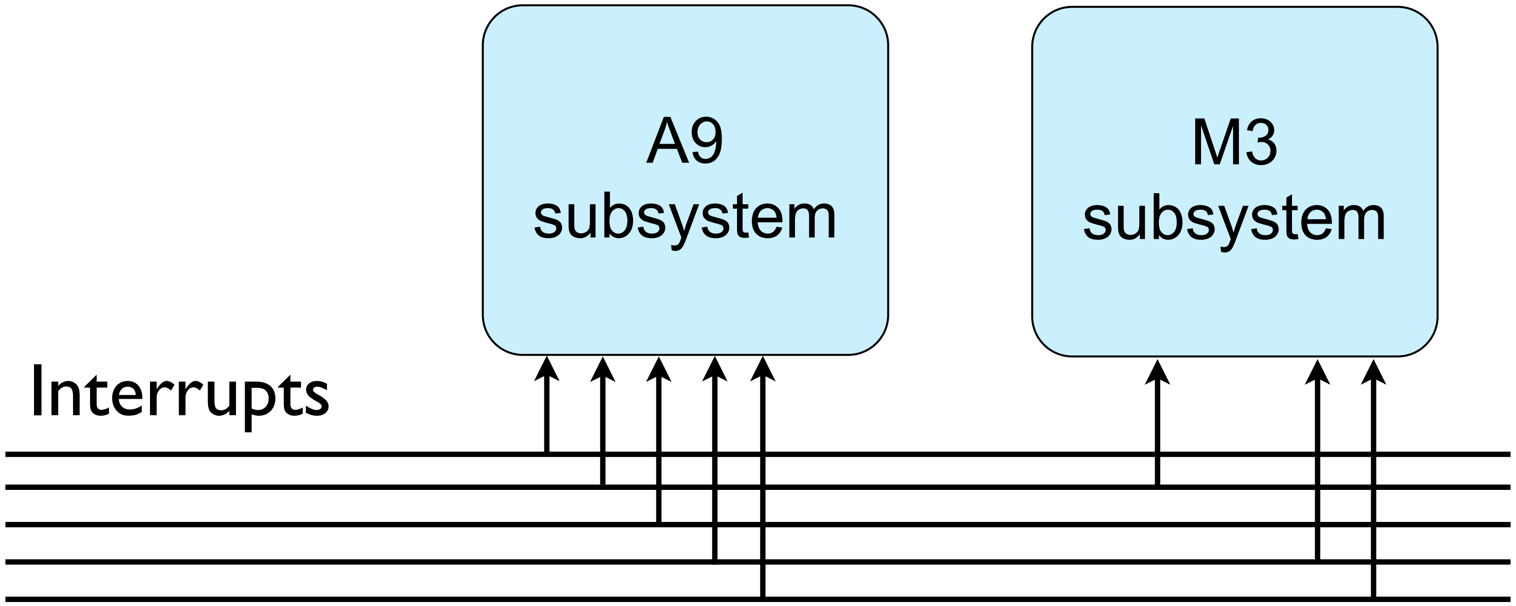
- Interrupt controller
  - the M3 and A9 cannot access each other's interrupt controllers
  - masking certain interrupts can only be done on certain cores
  - interrupts are not easily distributed, some interrupts are not mapped to the M3 subsystem



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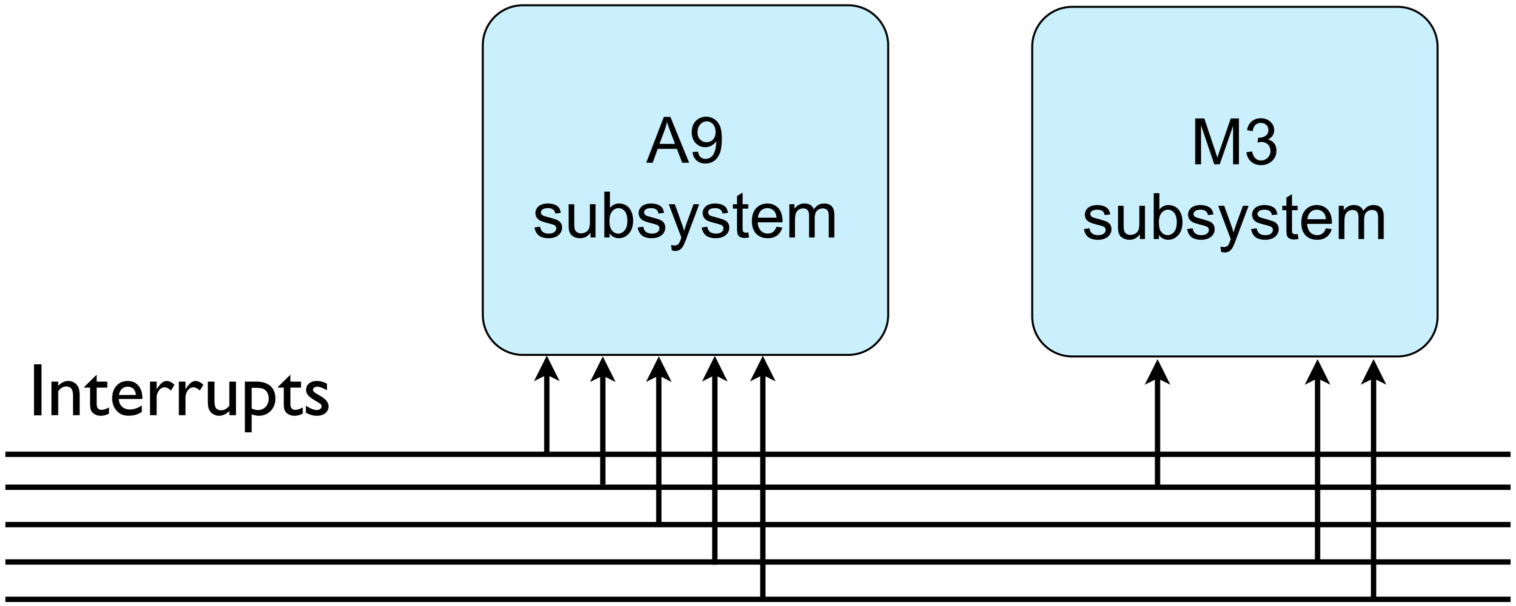

- This means that Linux can not completely run on the M3.

Now, Linux runs with both the M3 and A9, and we can migrate tasks between them!

Awesome! But what about performance?

- Investigate the overheads of our changes
- EEMBC
  - embedded benchmarking suite
  - wide range of workloads
    - automotive
    - telecommunications
    - networking
    - ‘consumer’

Awesome! But what about performance?

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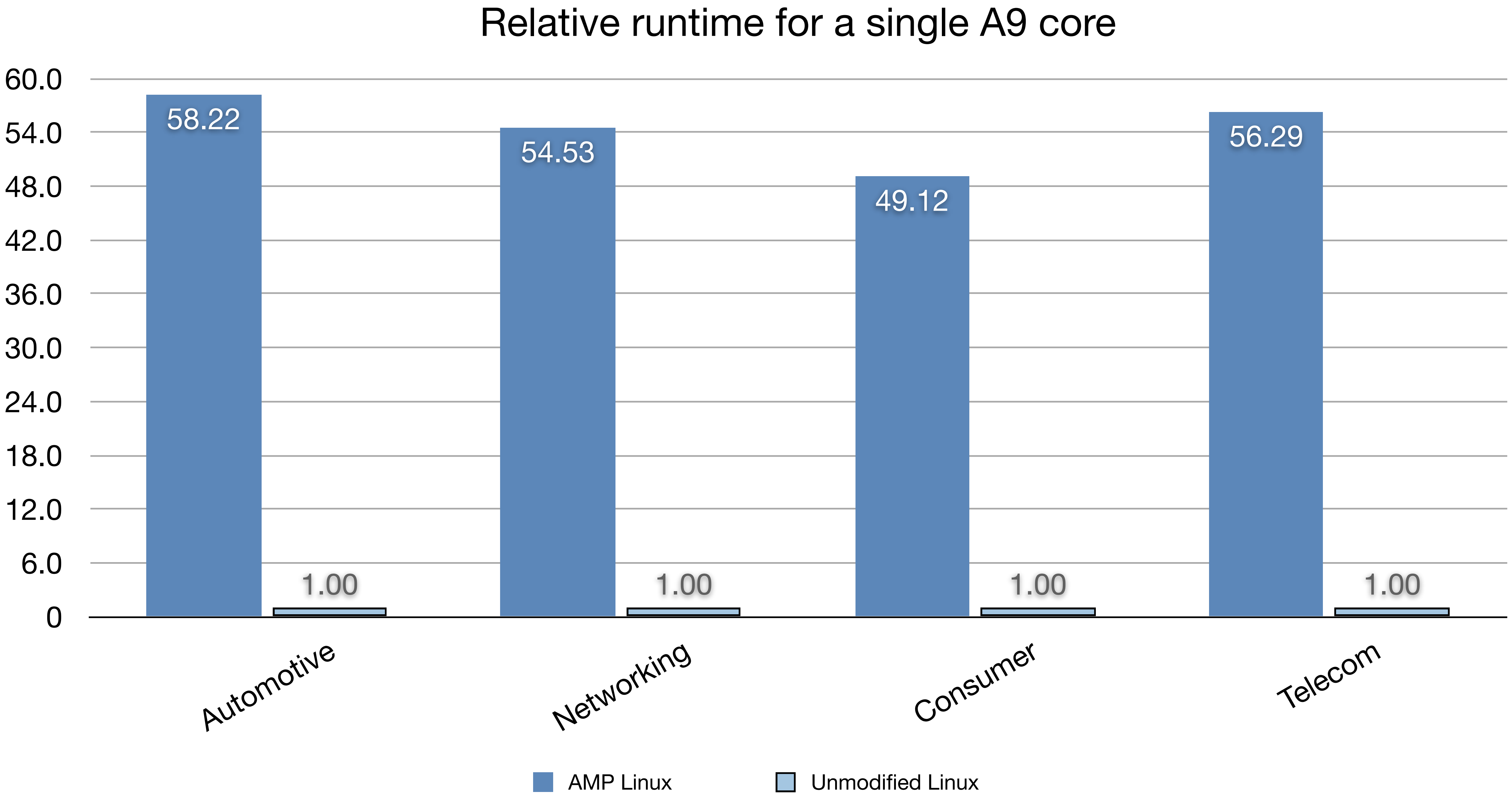
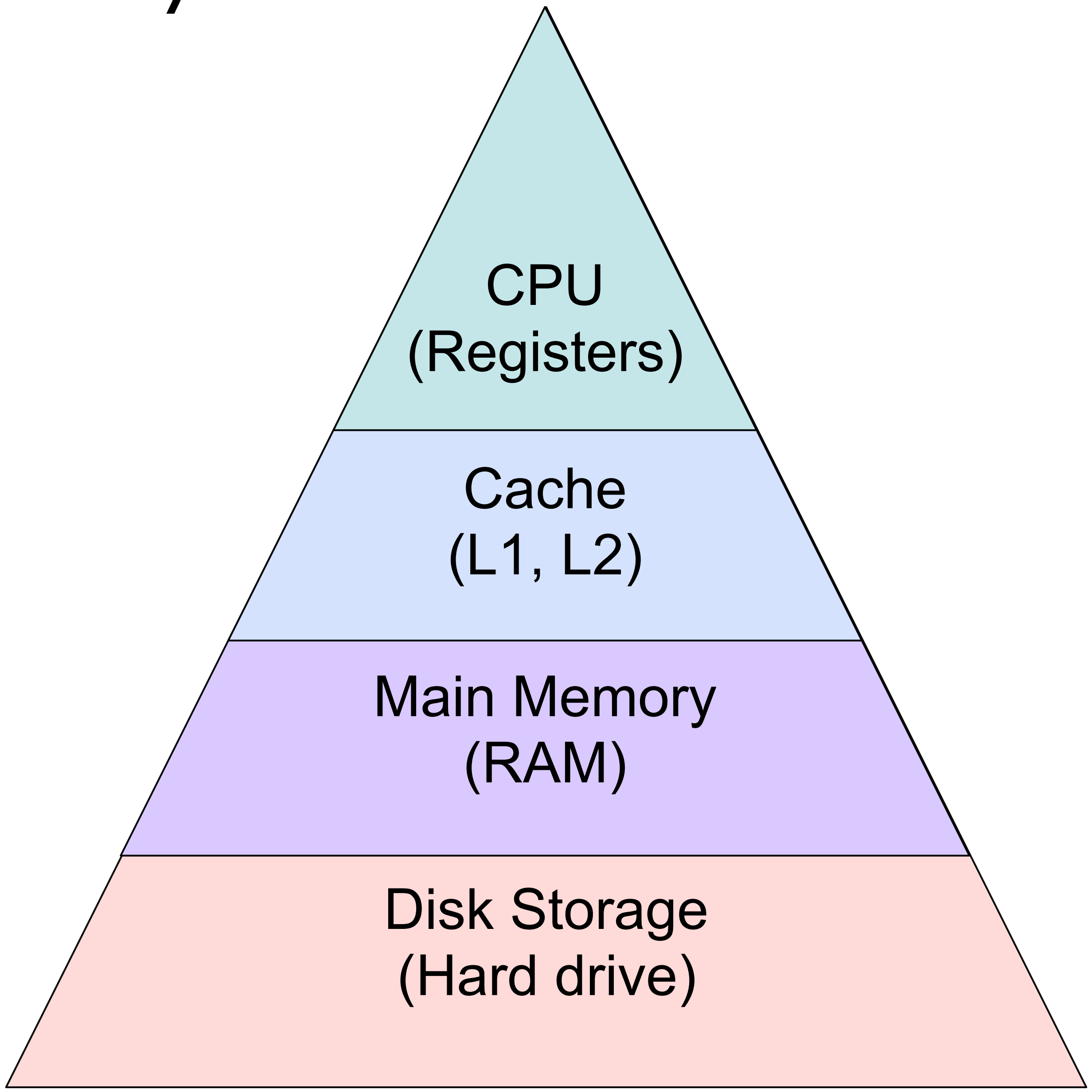


- Performance is *really* bad

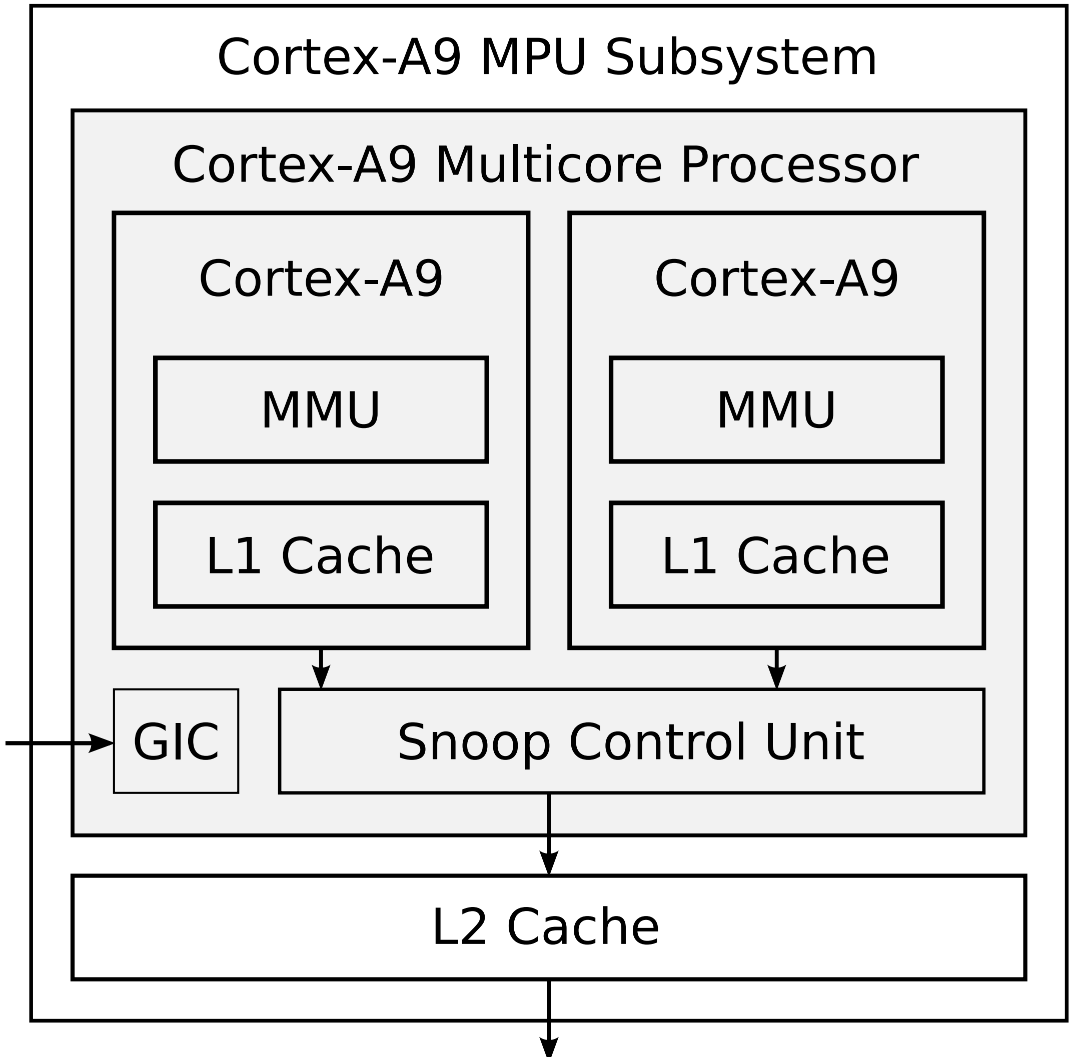
Caches are off!

- Caches provide improved latency



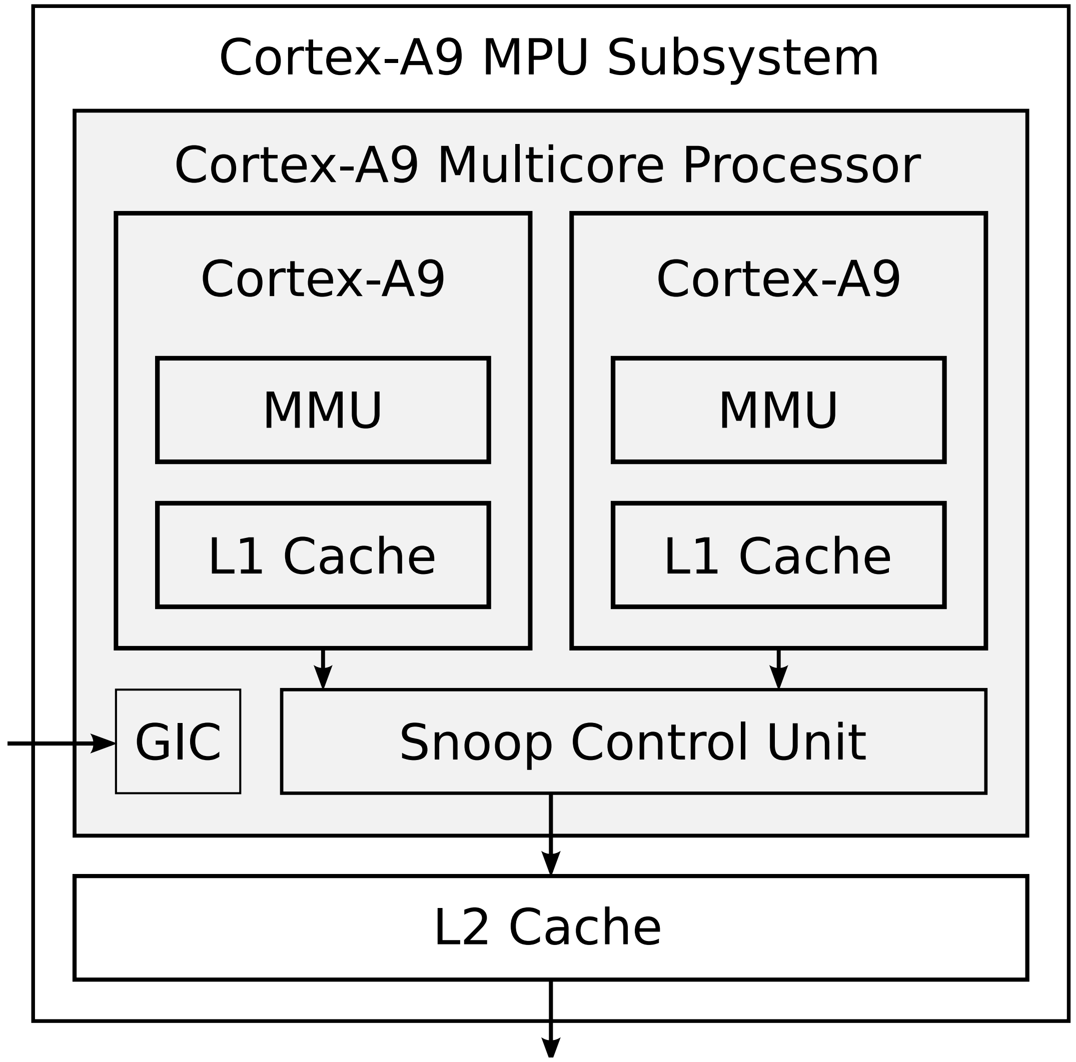
Caching on a multi-core system

- Shared caches
  - high latency
  - shared memory
- Local caches
  - low latency
  - less cache per CPU
  - cache coherency issues
- Combination



Cache coherency

- Sharing memory
  - out of date data
  - notify other cores of changes to data
- Cache coherency protocols
  - snooping (MOESI protocol)
    - requires hardware support



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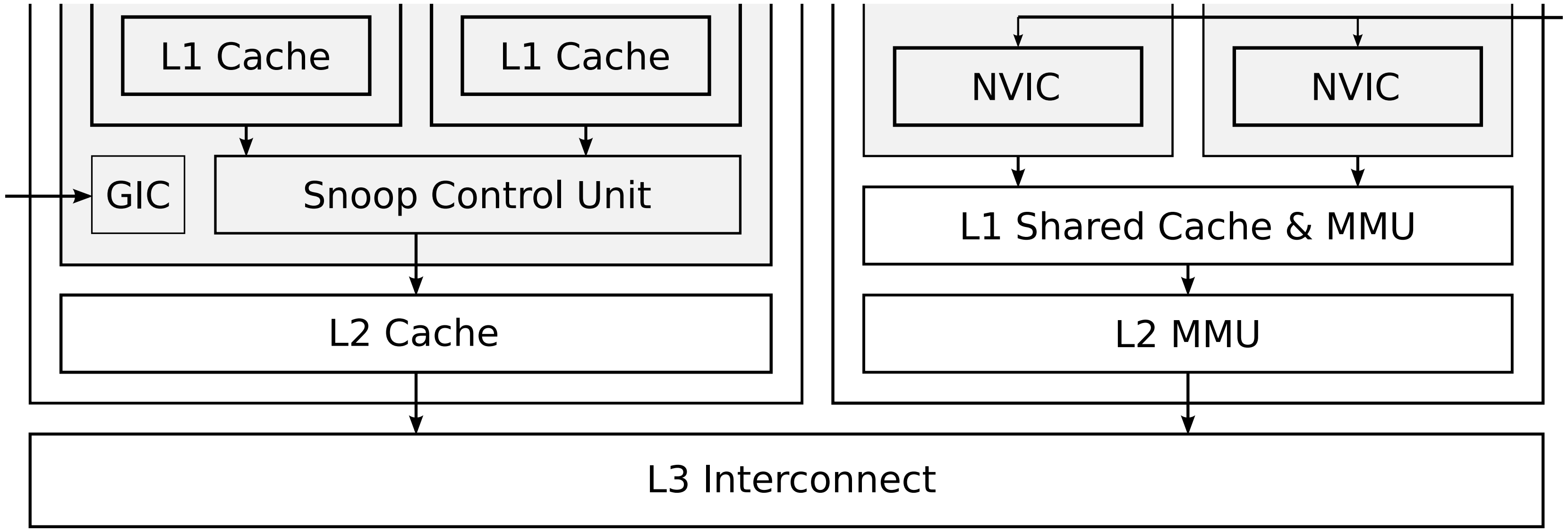

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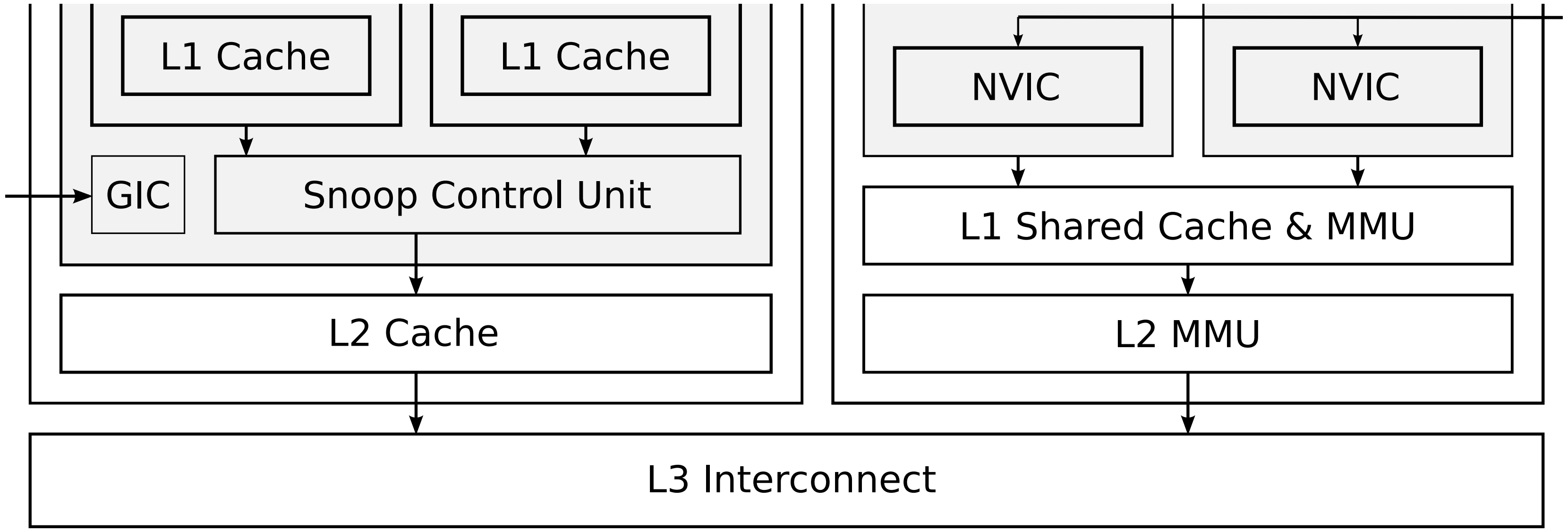

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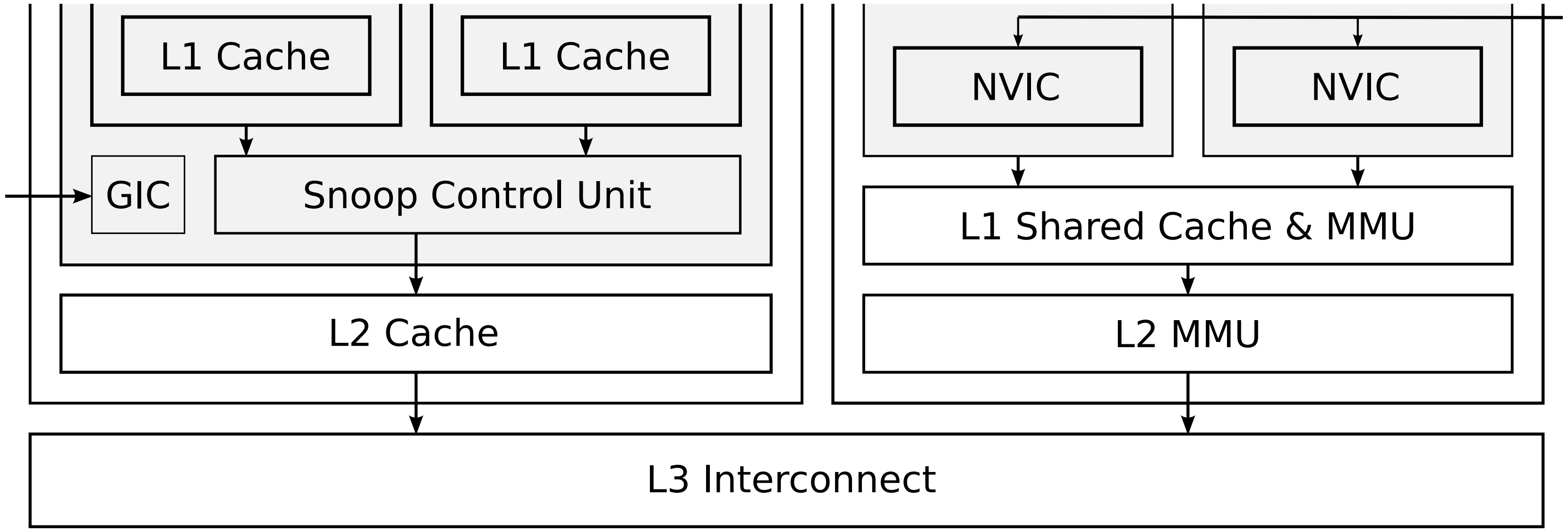
  - – sharing must occur at main memory
- No hardware support for cross-subsystem cache coherency
  - – efficient cache coherency requires hardware support (snooping)



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  - interrupt for signalling contention

Now we have caching!

Lets ignore the BKL for now ;-)

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- Compare performance of **just** an A9 core
- Vary what the M3 core is doing

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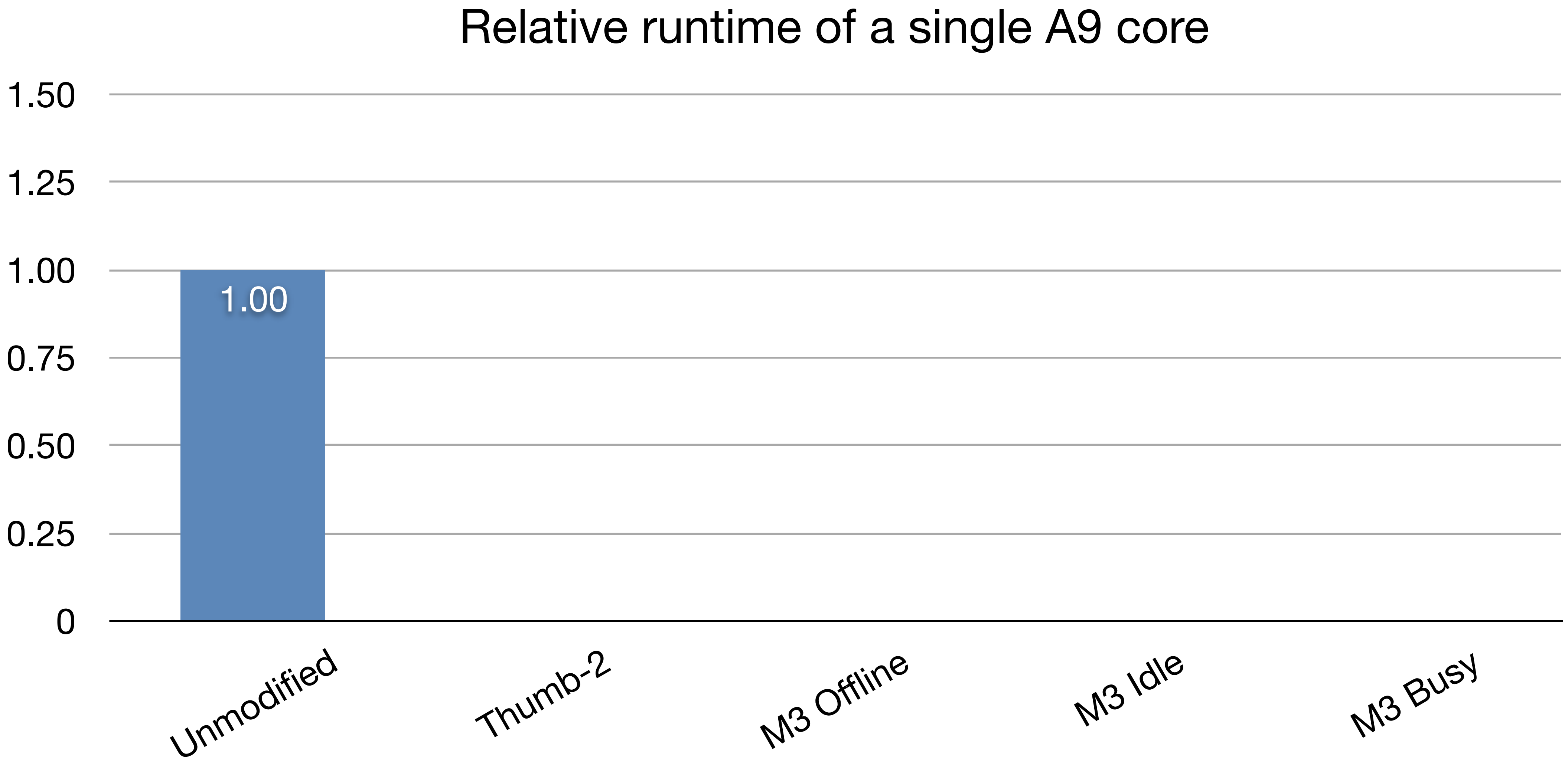

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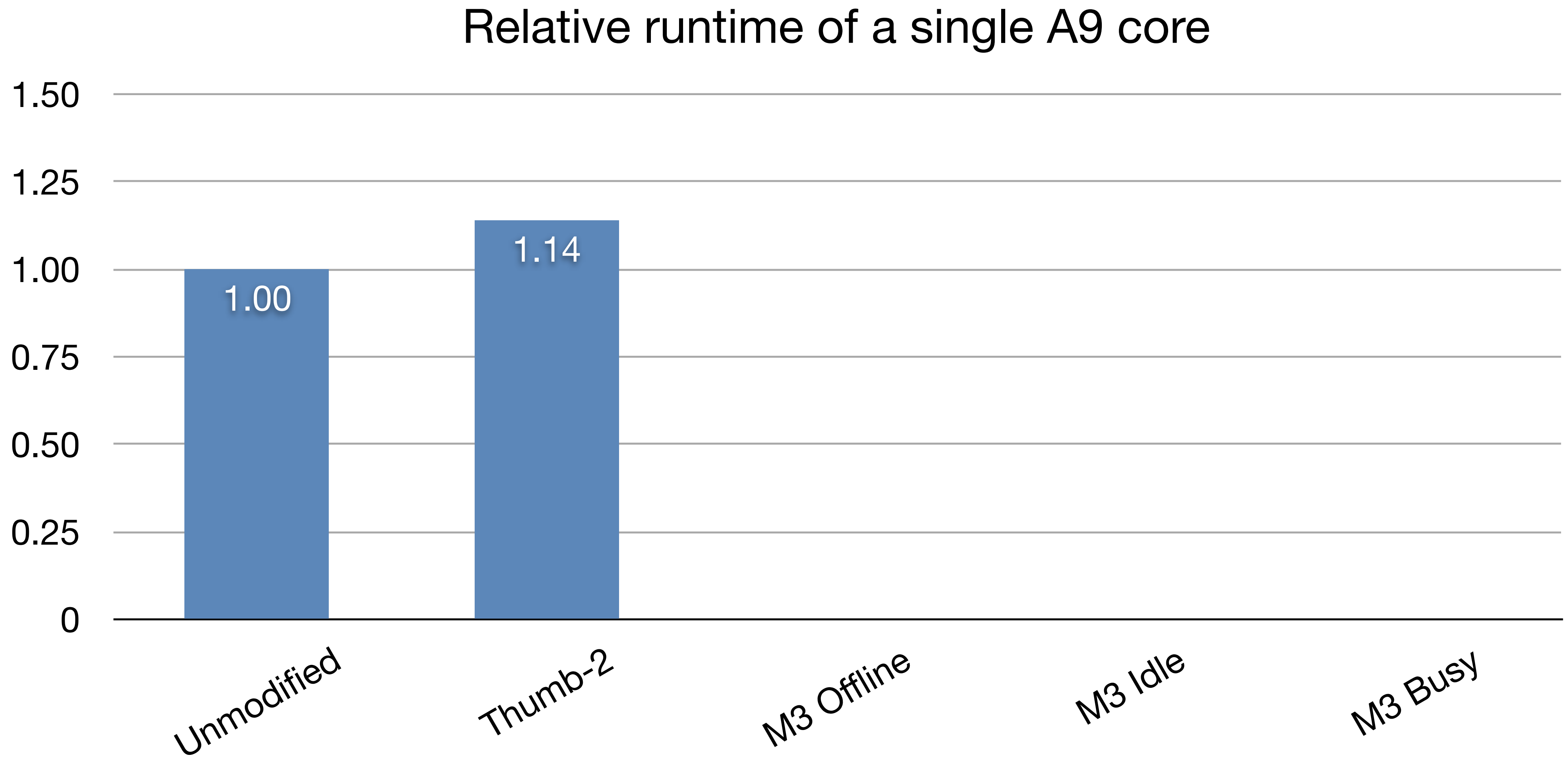

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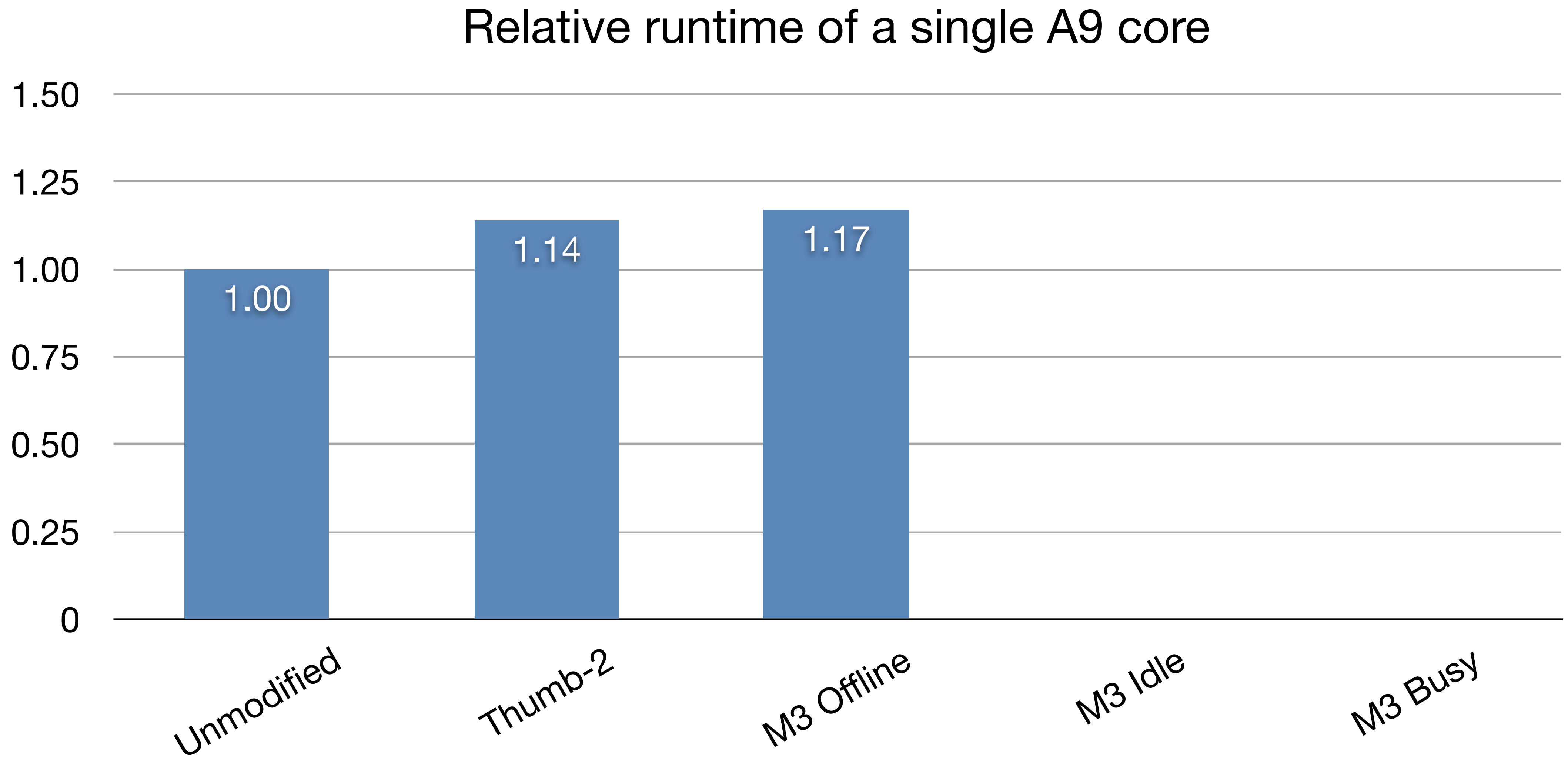

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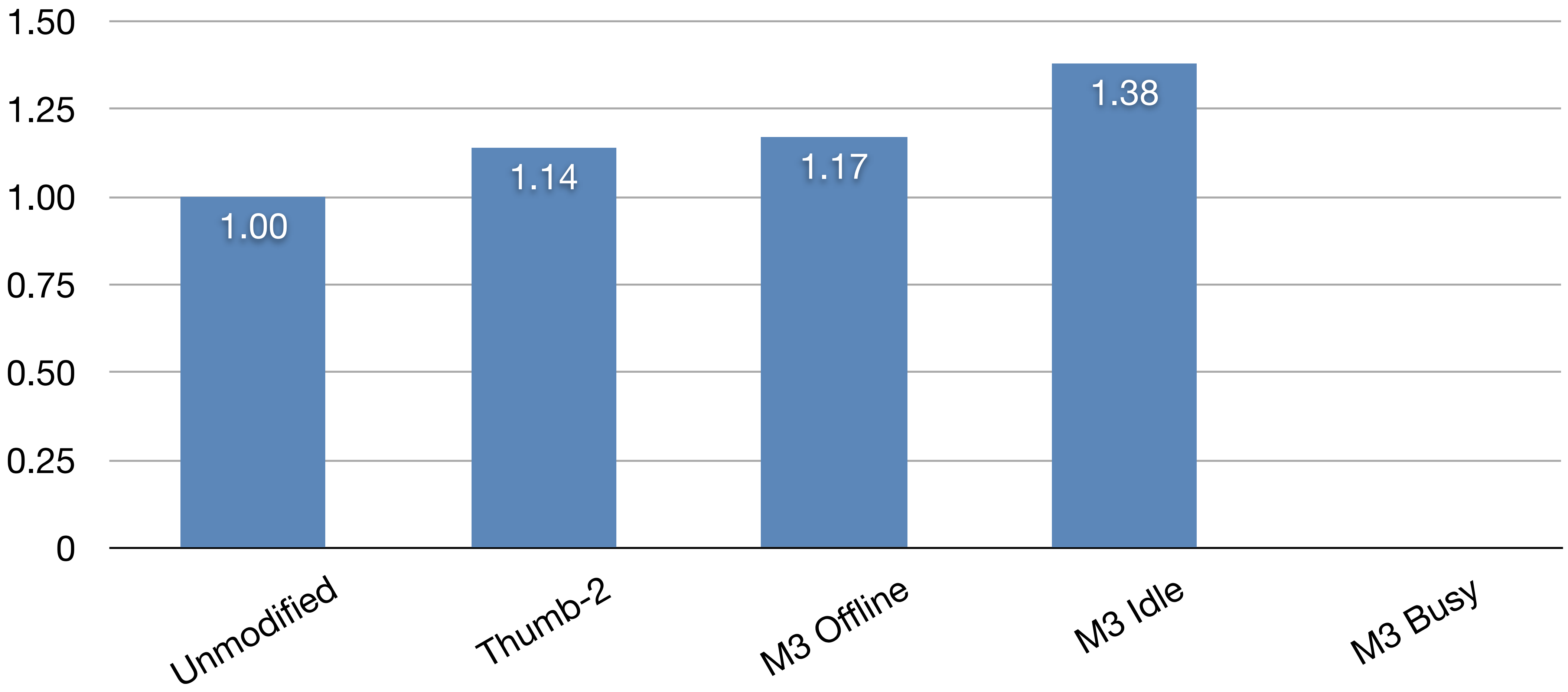
Relative runtime of a single A9 core



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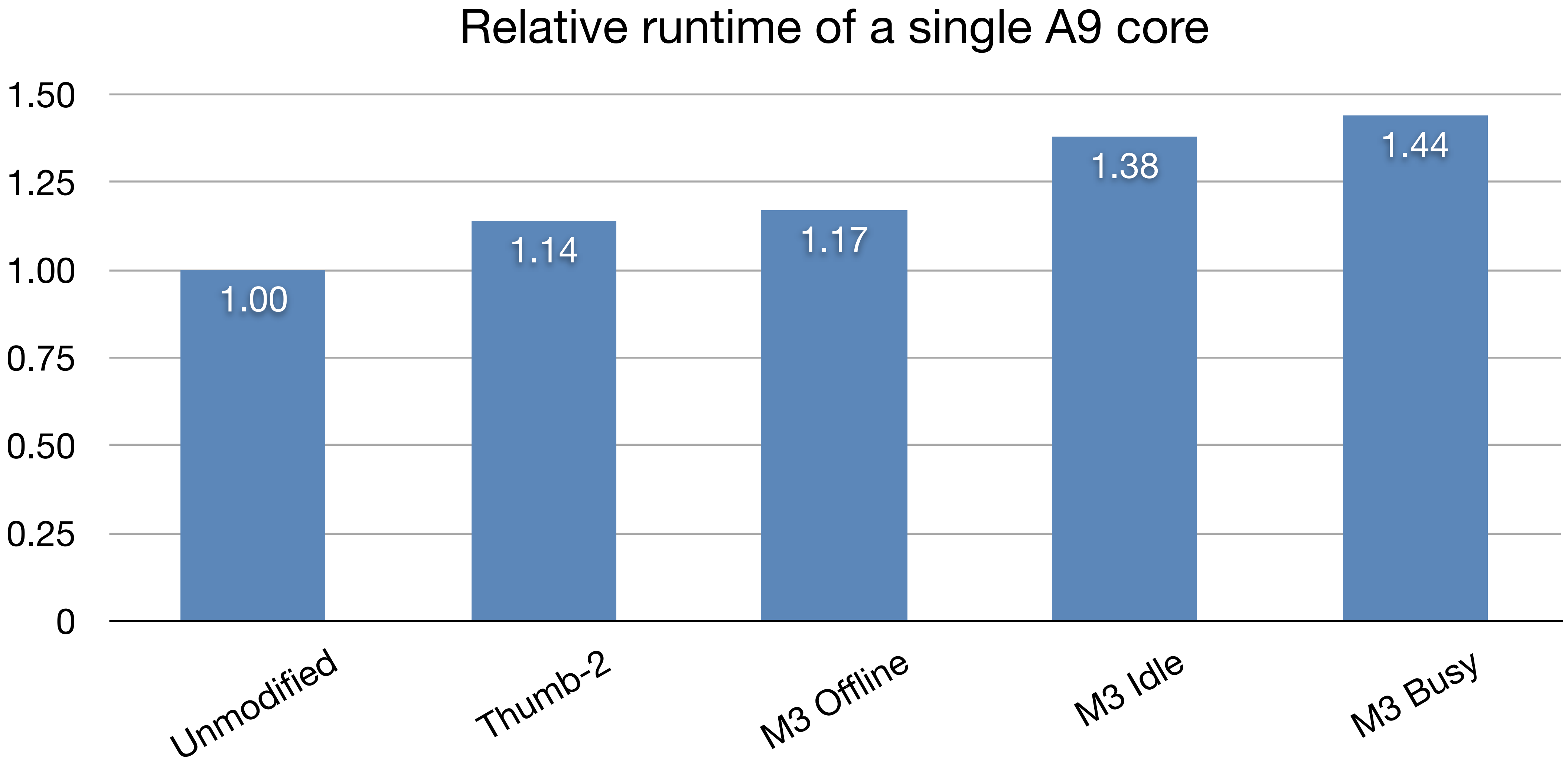
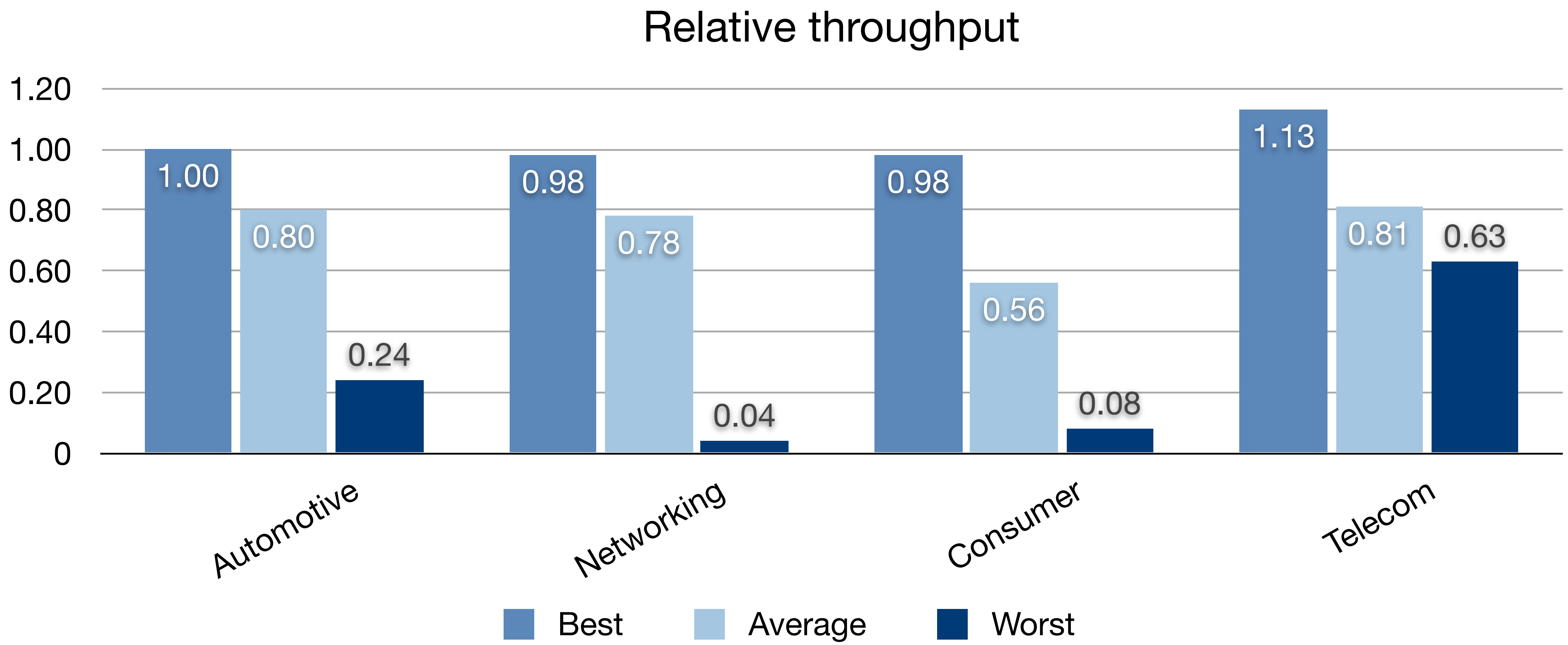


System throughput

NICTA



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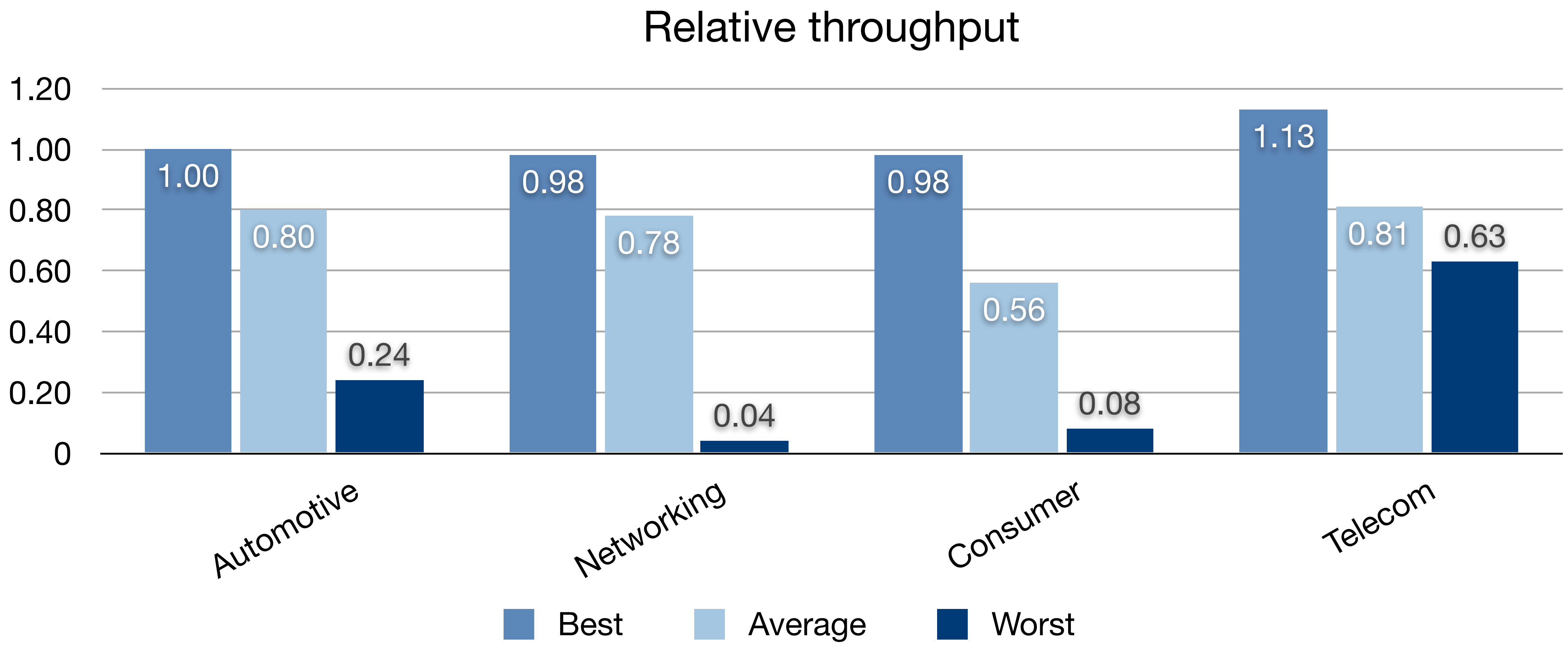
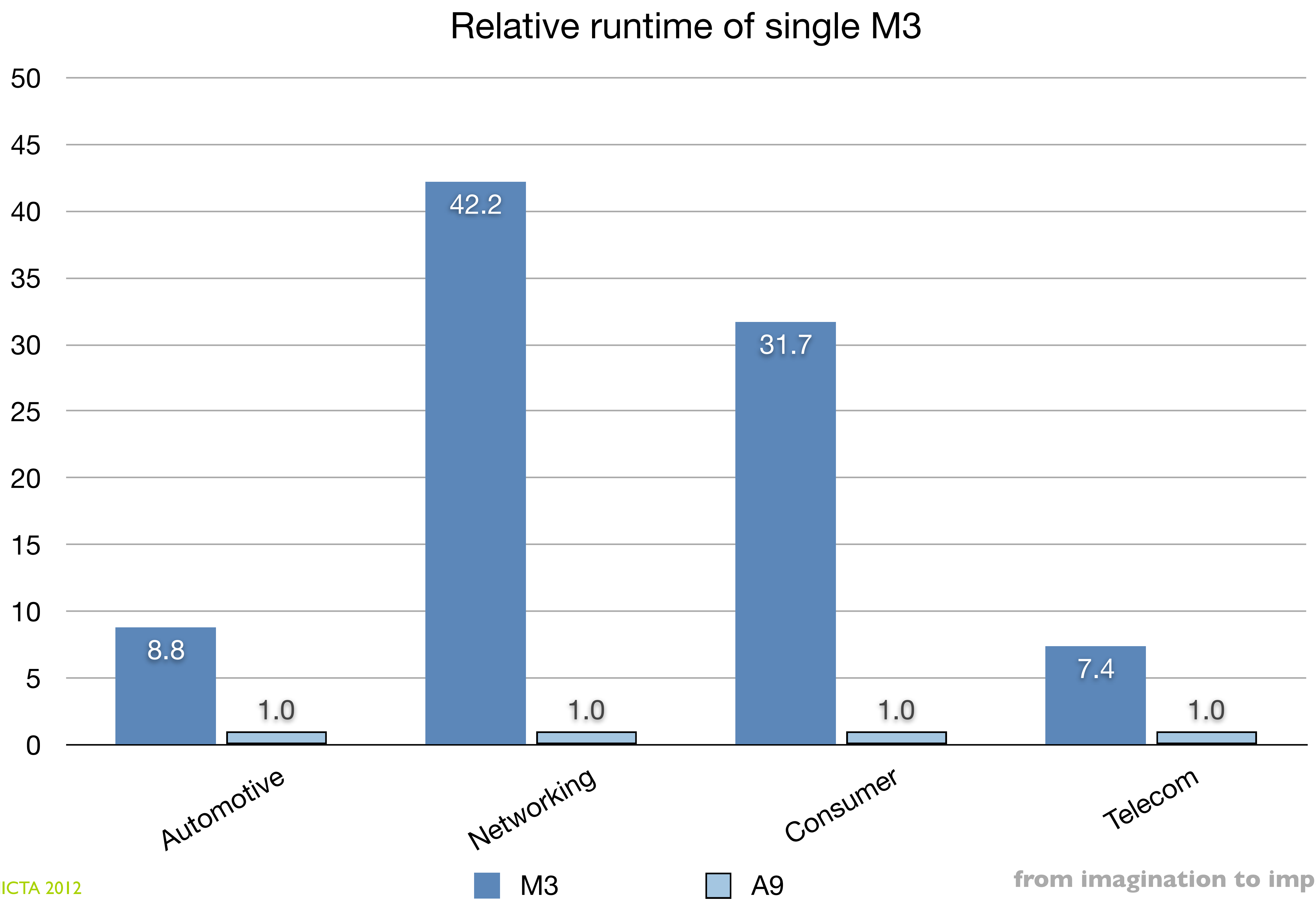


- Performance is still not great
  - M3 doesn't make up for overheads
  - worst case due to high L1 TLB (software loaded) miss rate, as the M3 spends most of its time refilling the L1 TLB, locking the A9 out of the kernel

Using the system

M3 vs A9

NICTA



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- Can energy-efficiency be improved by using the M3s?
  - performance overheads negate any savings
- How can the system know how each core will perform?
- How can scheduling decisions be made?

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- Decide whether it's worth migrating...
- Prediction is within about 10% error for a wide range of workloads from EEMBC

Conclusion

- Linux can now schedule tasks on both A9 or M3 cores
  - overheads are high mostly due to lack of hardware support
  - with a bit of support from the hardware, the system should be usable
- With the right counters, performance prediction is accurate
  - again, hardware support would help, either provide performance counters on the M3s or better performance counters on the A9s.
- It only took 8500 lines to do.
  - No, we haven't pushed it upstream.
  - If you're interested in the details, look out for a potential Usenix ATC publication - fingers crossed.

Questions?

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From **imagination** to **impact**

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Expected Questions

- Will we push the changes upstream?
  - a lot of changes to linux for not much gain atm.
  - very specific to OMAP4430, which is not very useful.