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Formal Methods (FM), 7 March 2023

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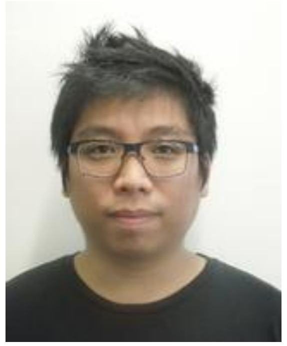
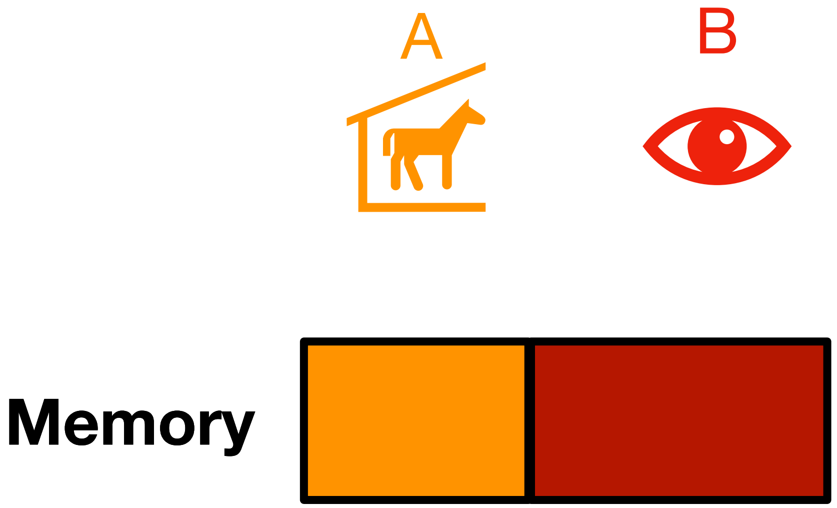
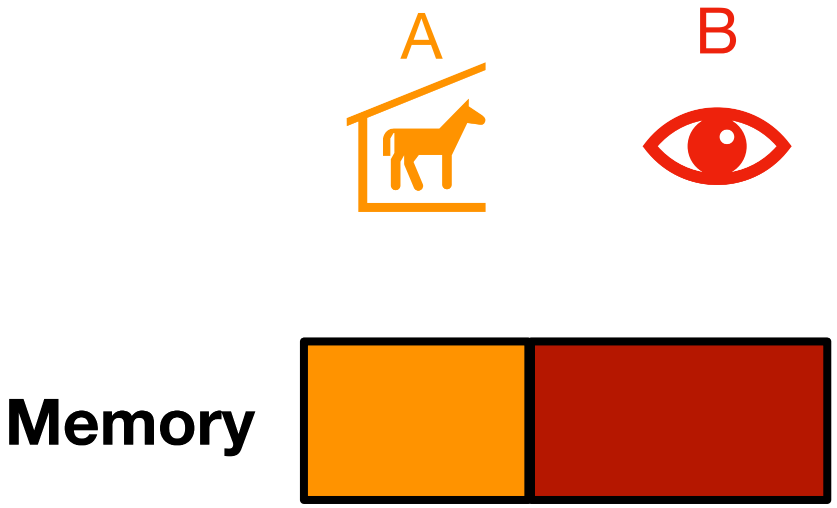


Threat scenario: *Trojan* and *spy*



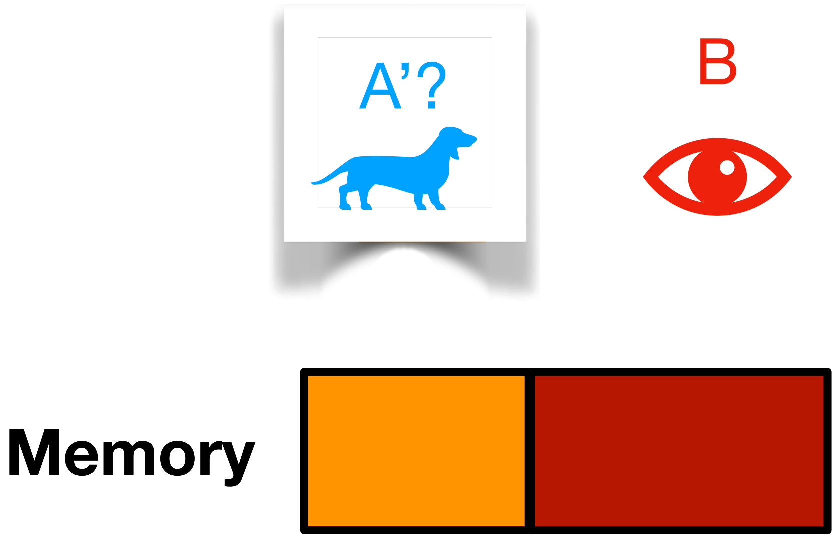
Threat scenario:
Trojan and *spy*

Covert channels



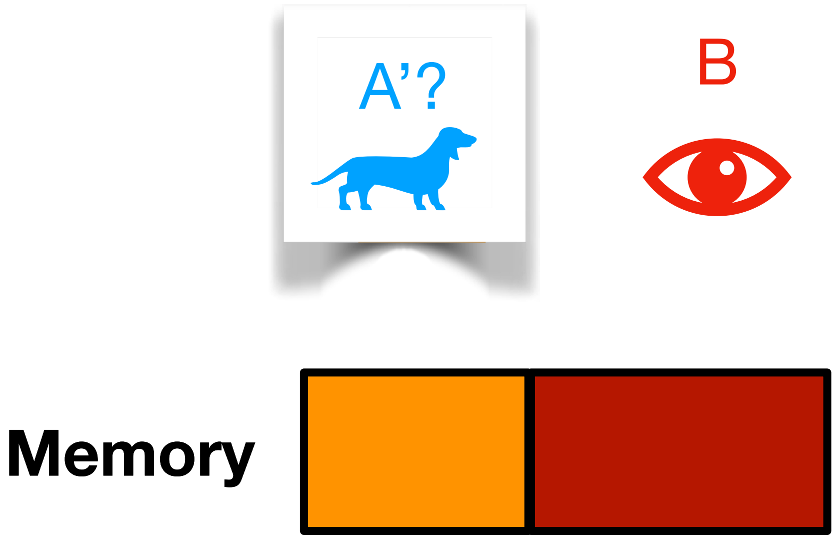
Threat scenario: *Victim/~~Trojan~~* and *spy*?

Covert channels
+
Side channels



Threat scenario:
Victim/~~Trojan~~ and spy?

Covert channels ✓
+
Side channels ✓



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Covert channels
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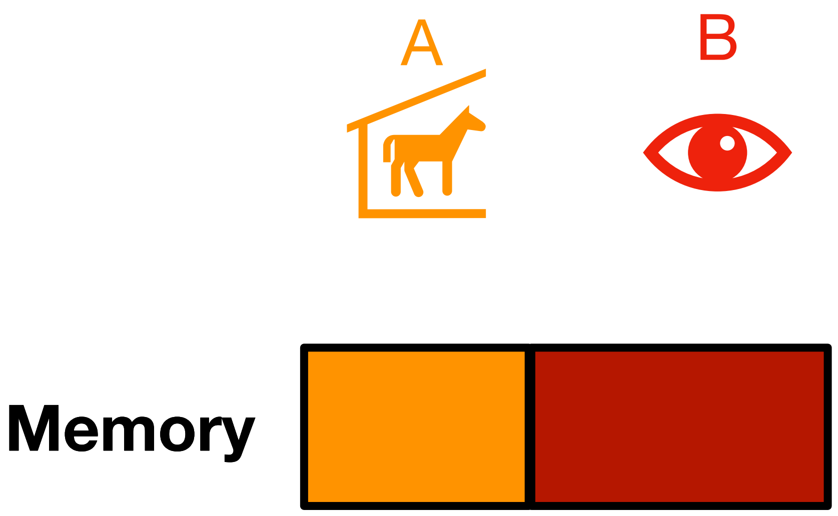


A

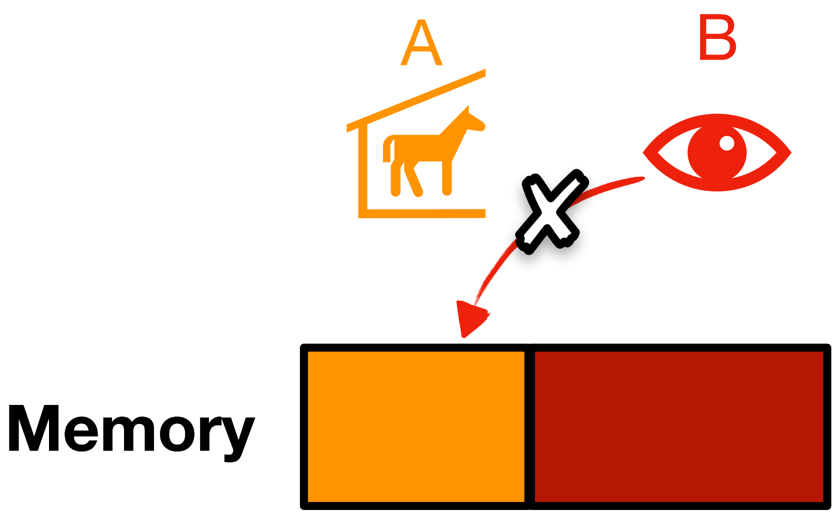
B

Memory

Threat scenario: *Trojan* and *spy*

Covert channels
+
Side channels

- OSes typically implement *memory protection.*



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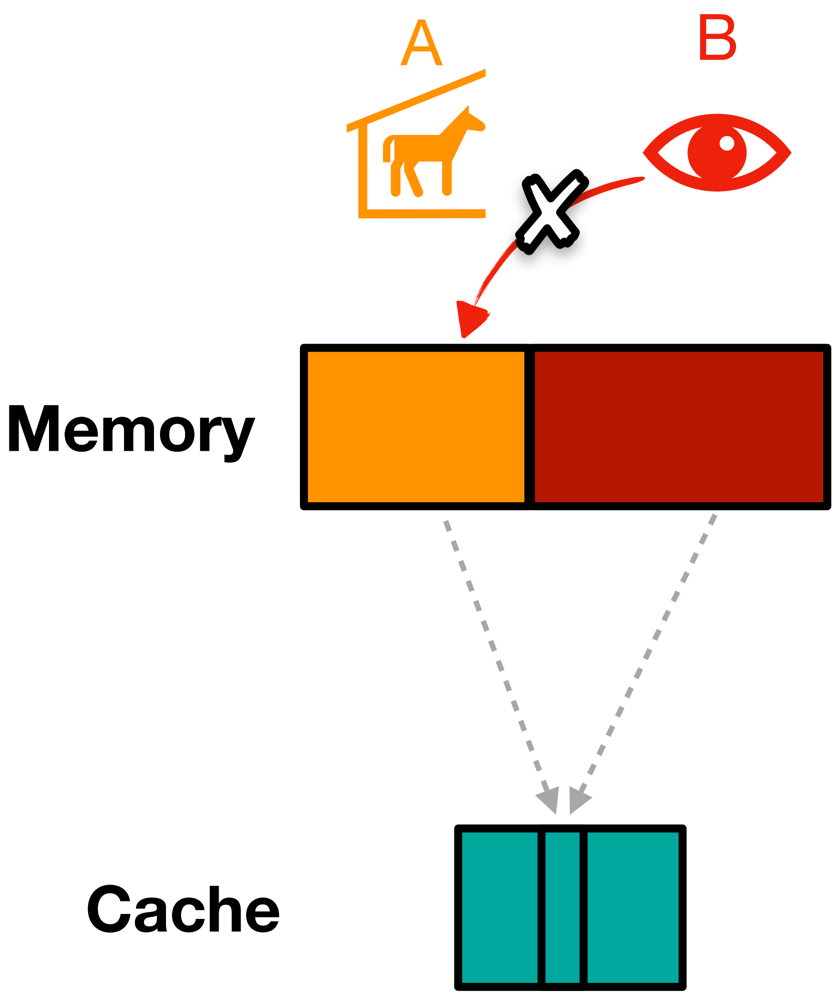

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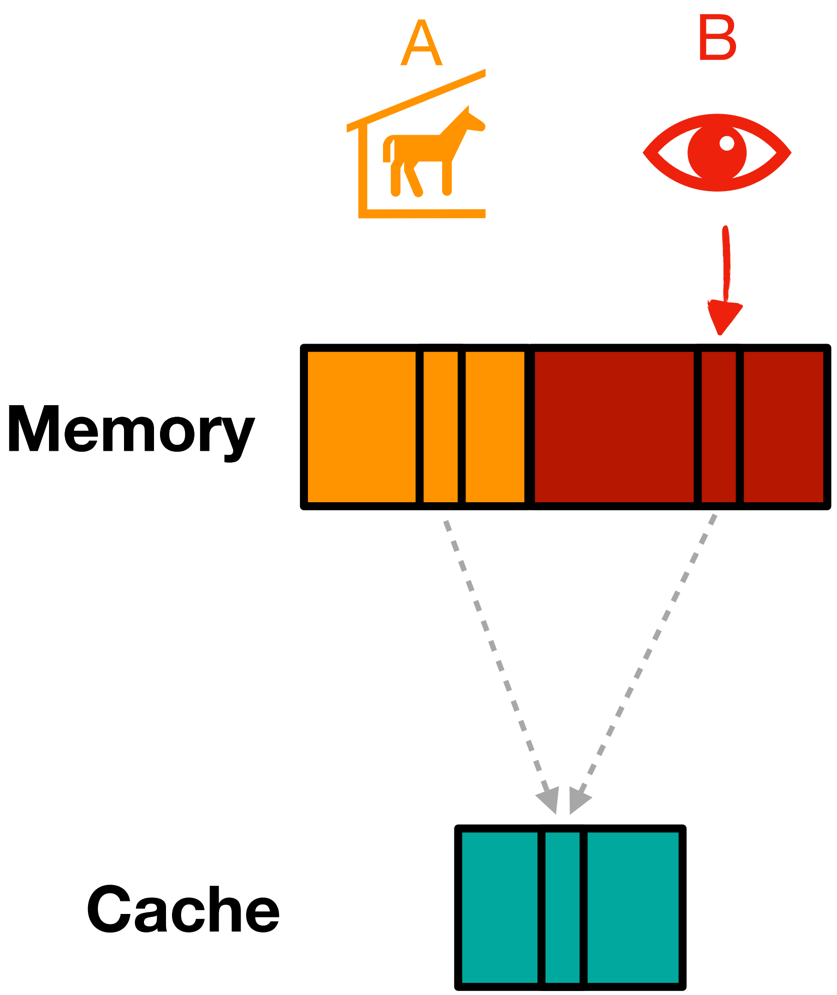

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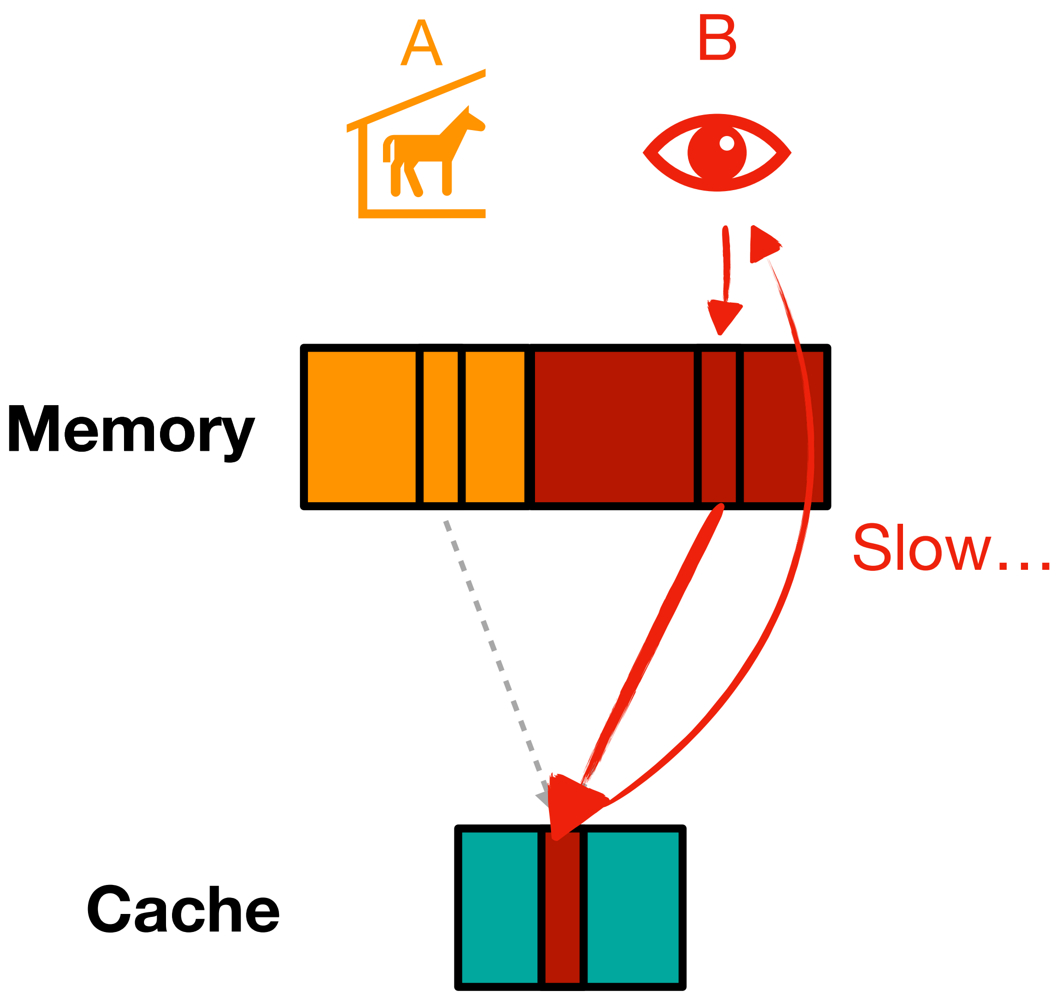

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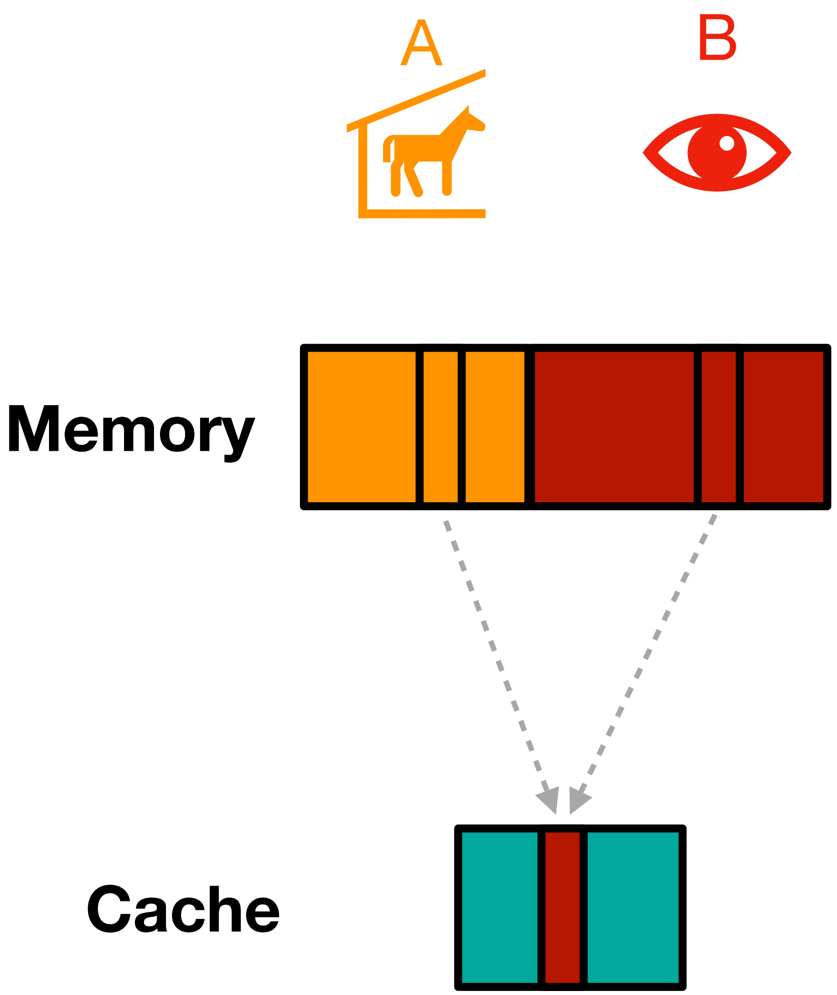

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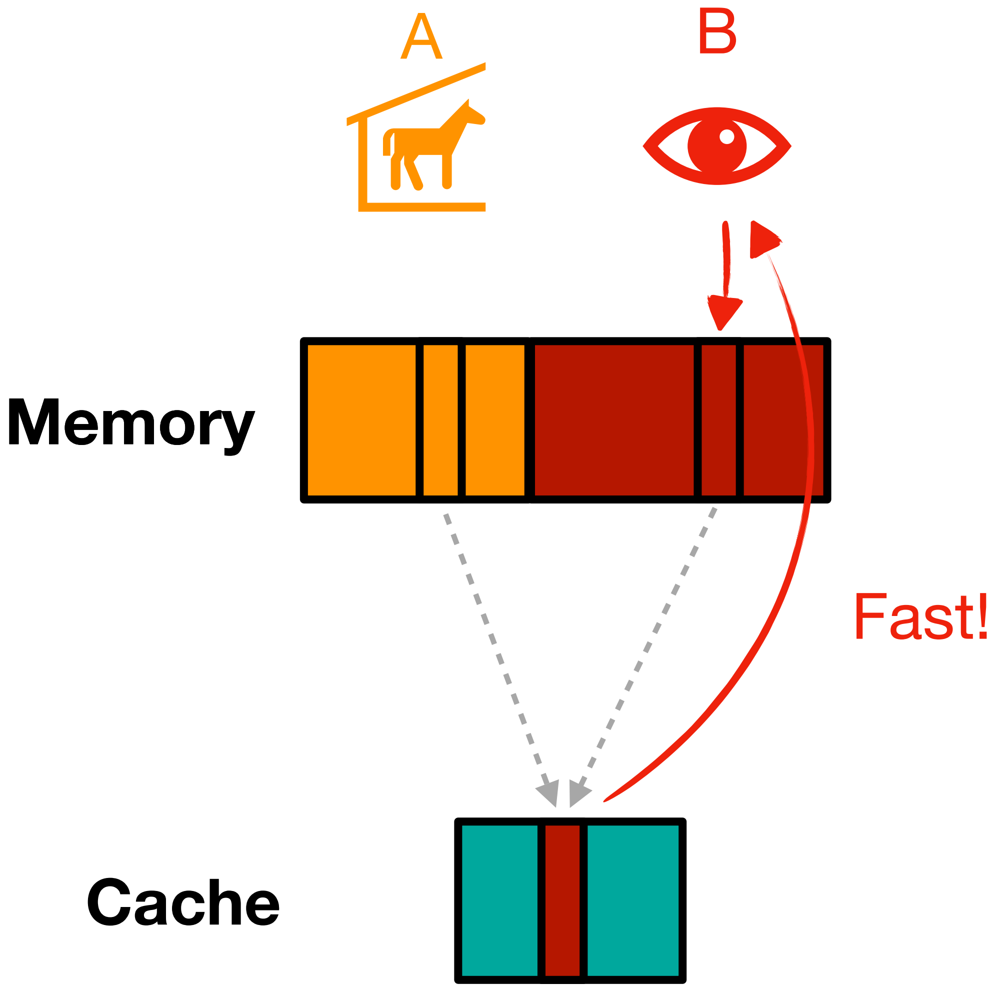

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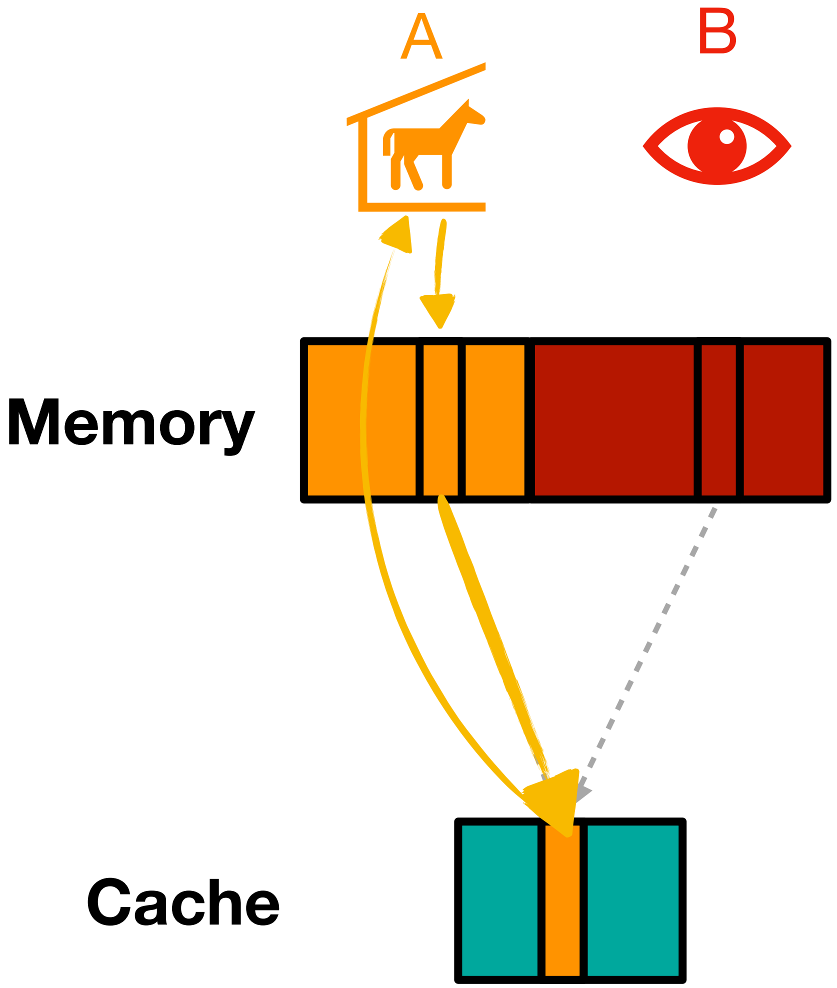

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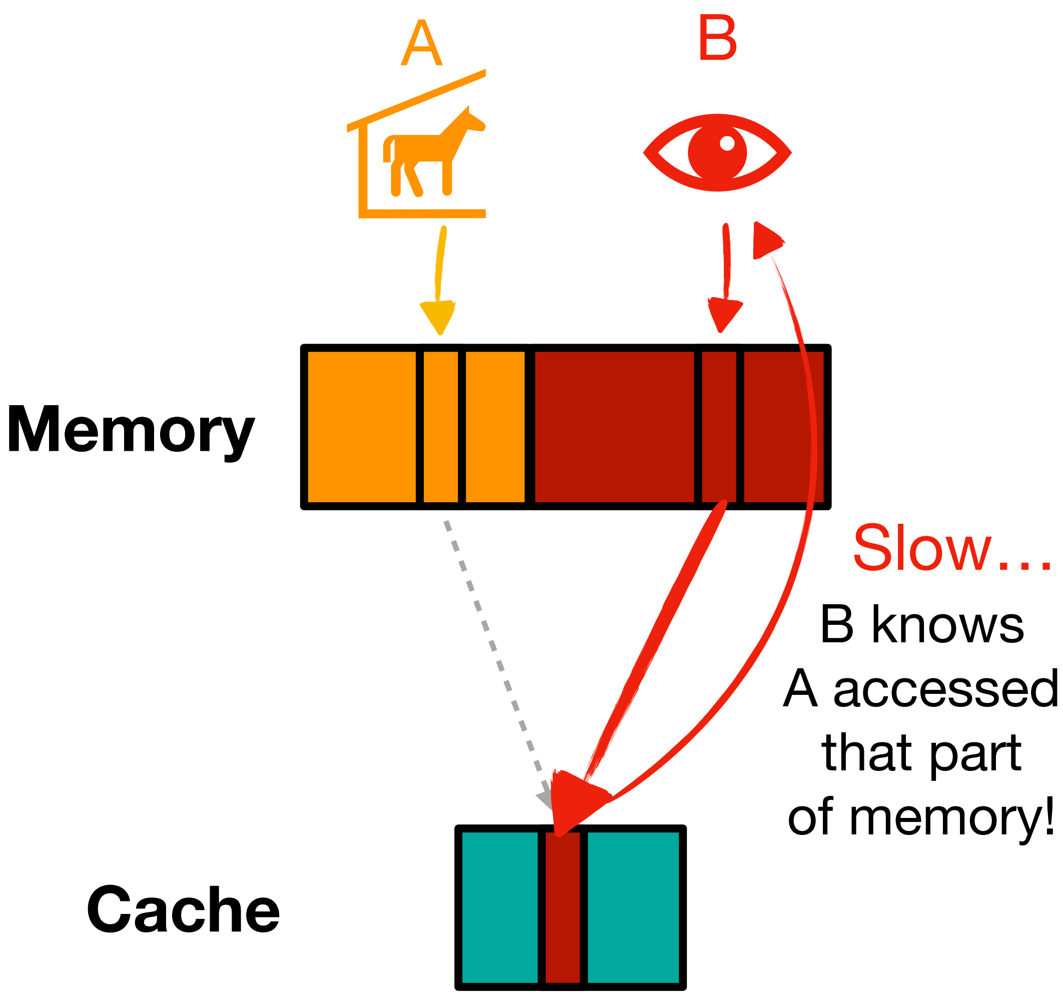

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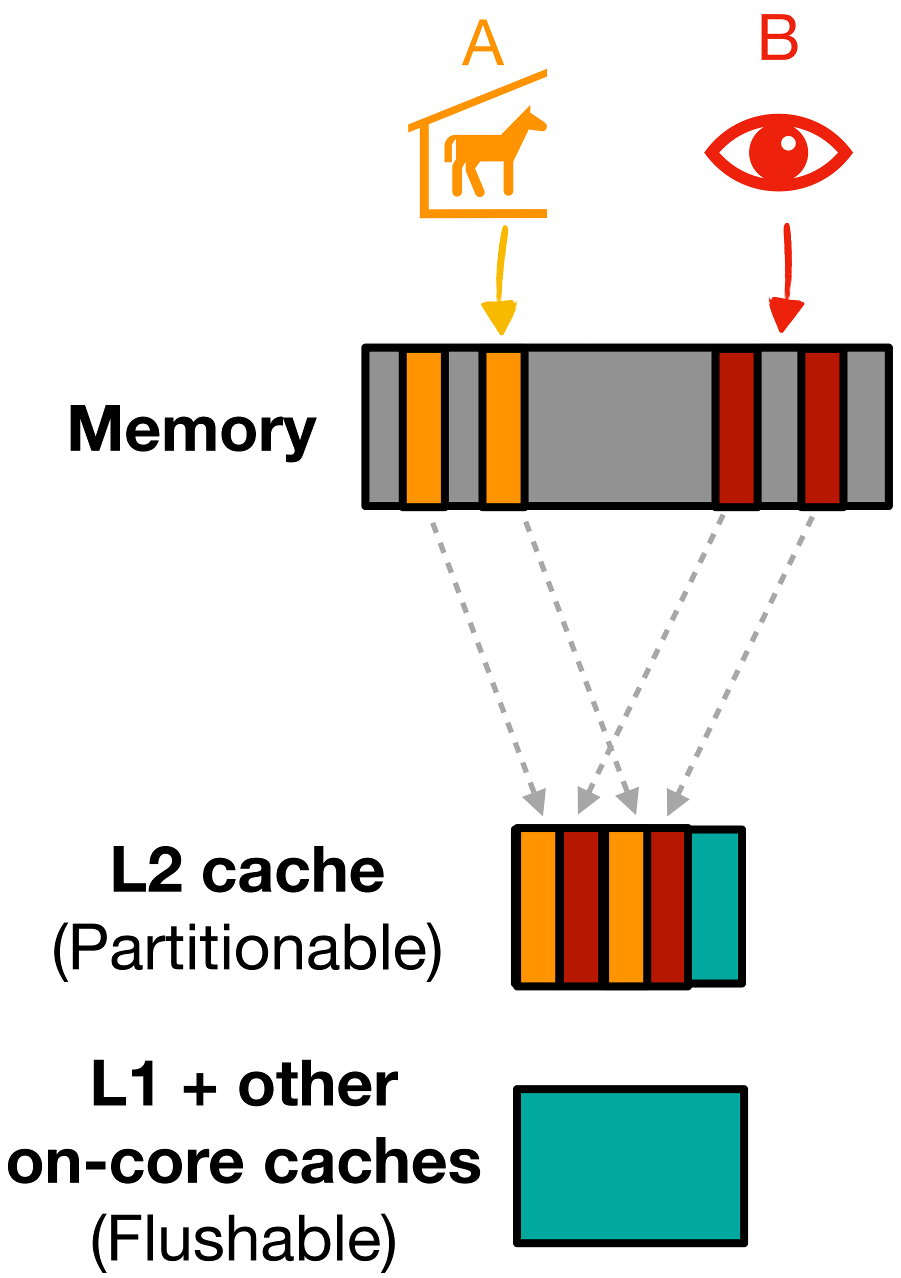
  e.g. [Ge et al. 2019] for seL4 microkernel OS
  - Partition what we can
  - Flush what we can't



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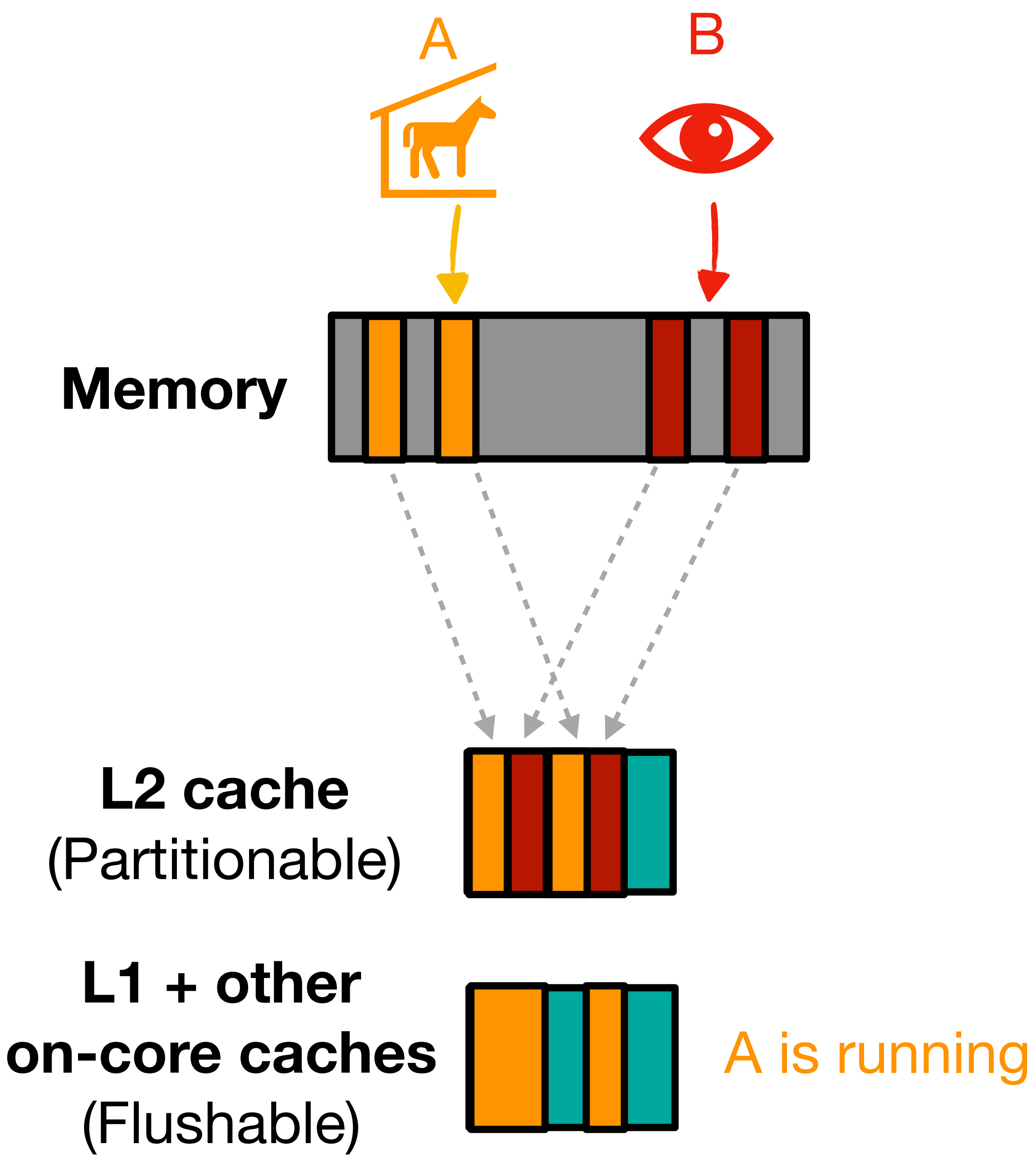

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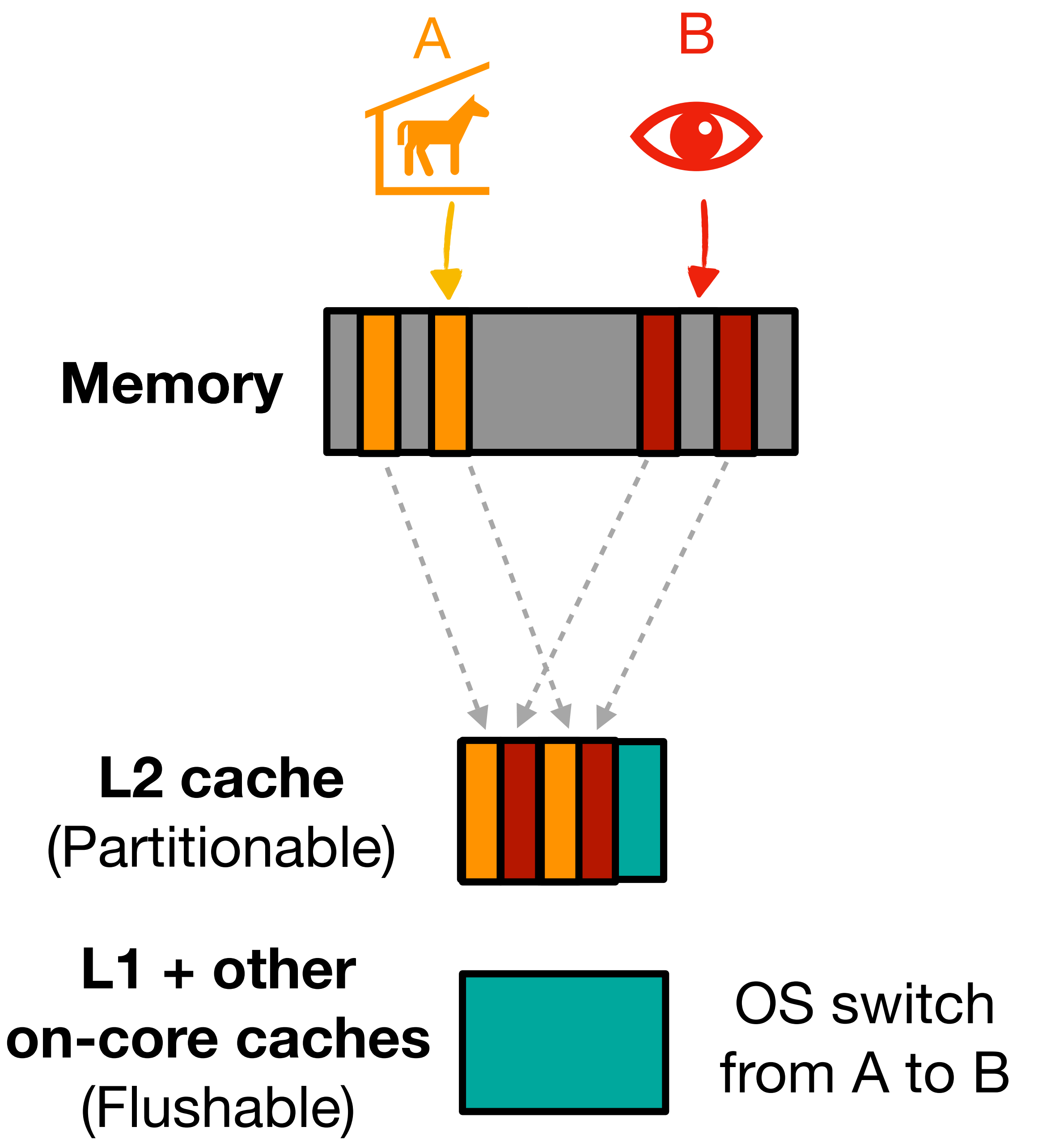

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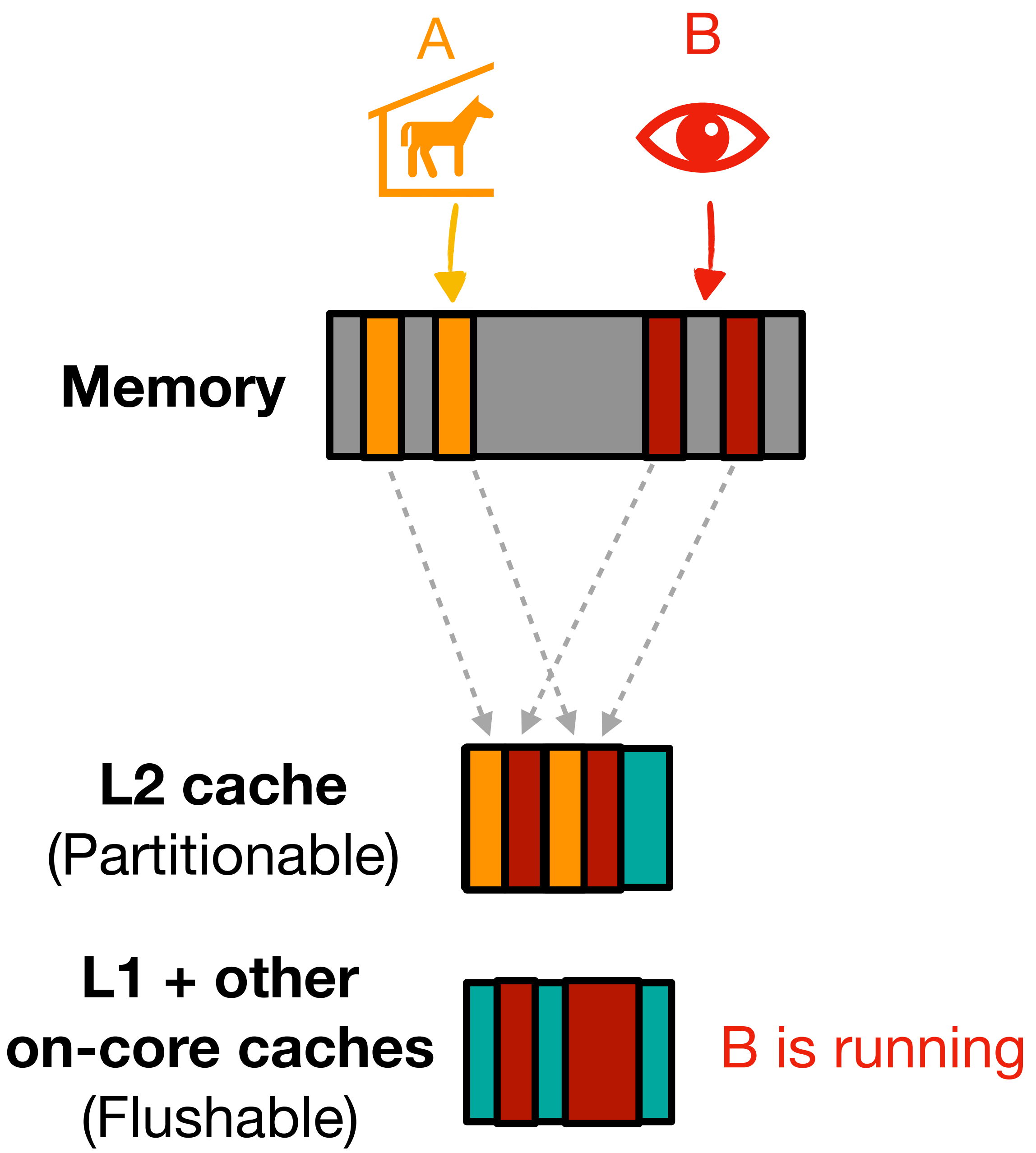

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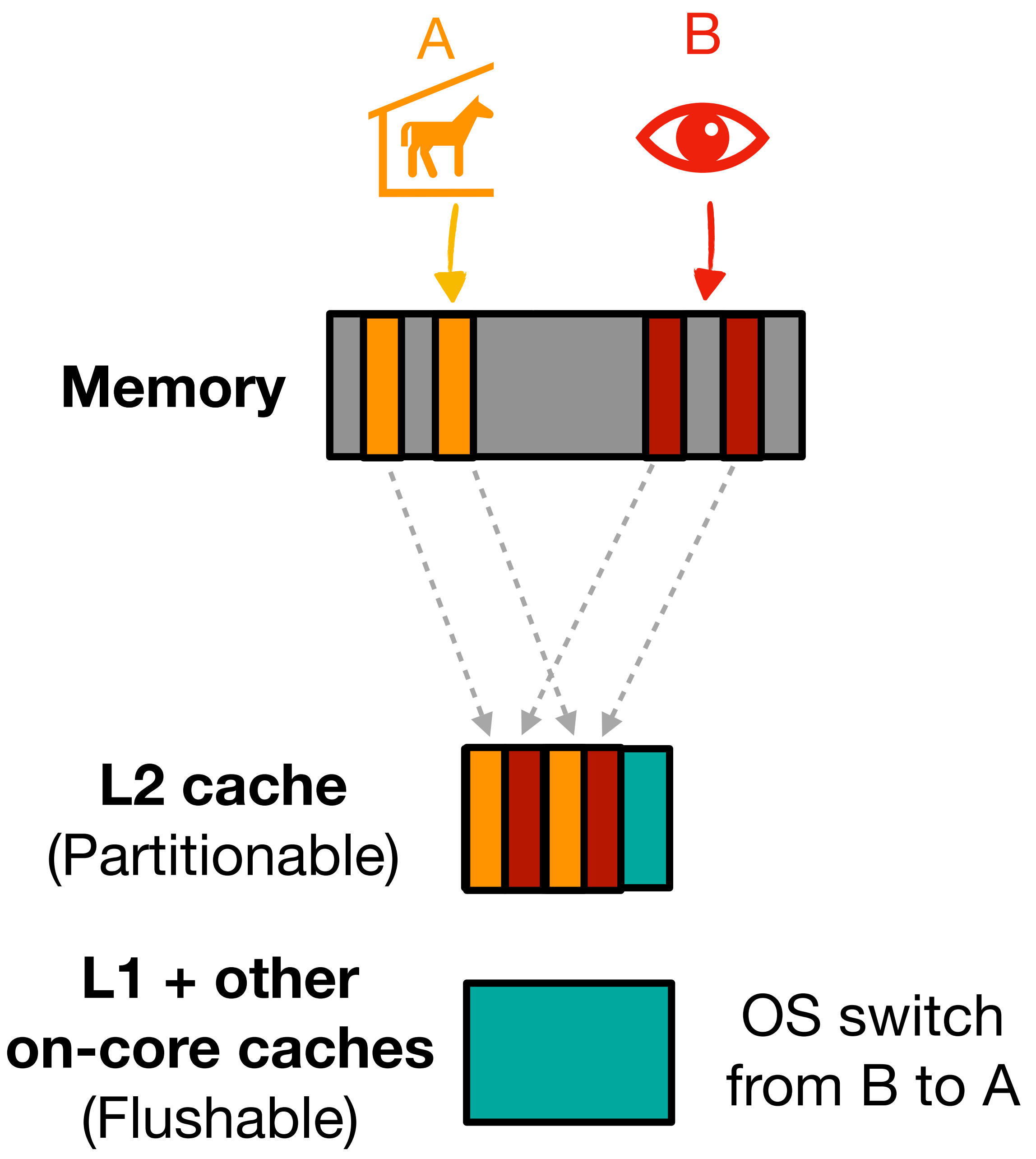

A

B

Memory

L2 cache
(Partitionable)

L1 + other on-core caches
(Flushable)

OS switch from B to A

"Flush": Write fixed content; wait up to fixed time.

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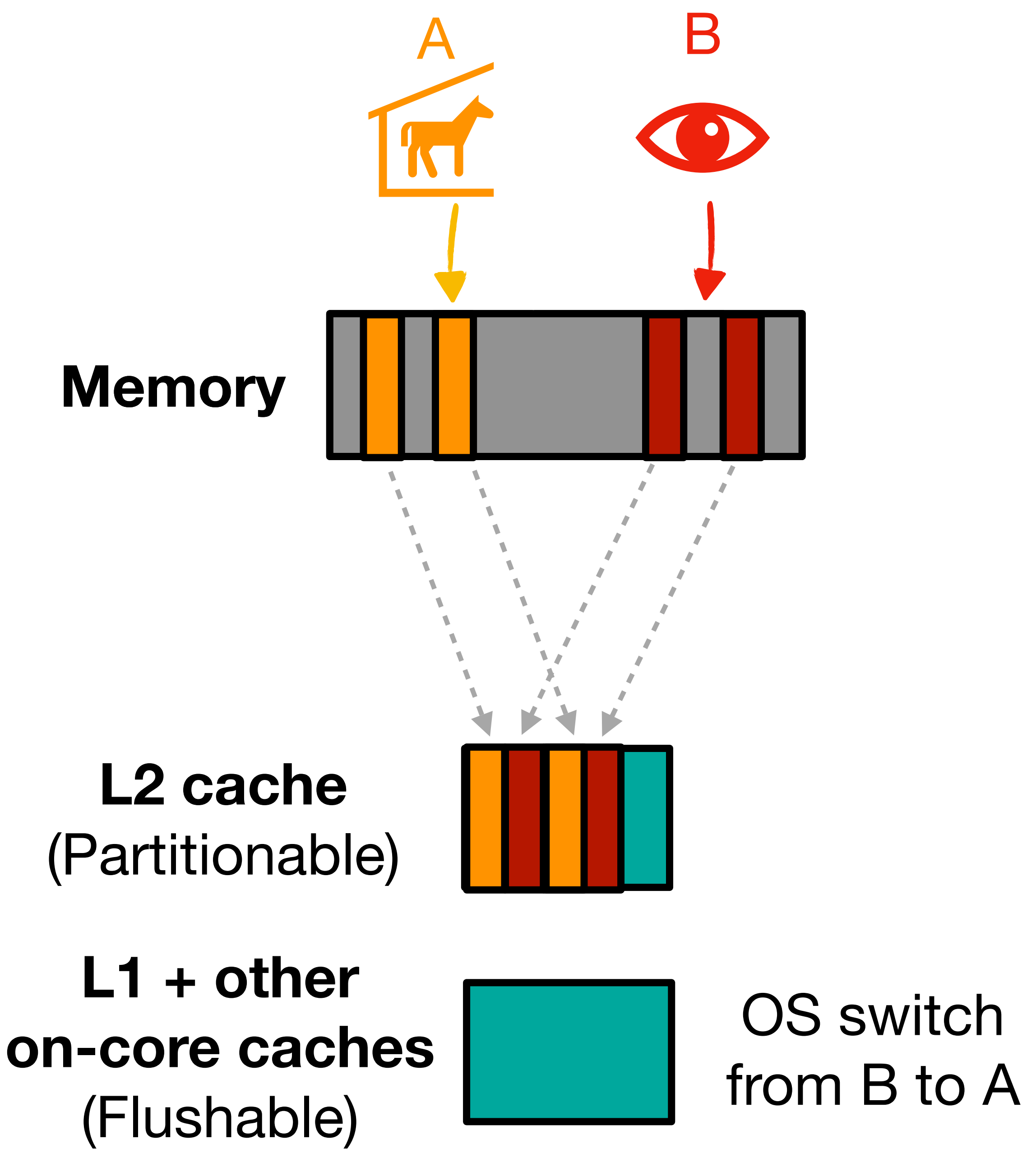
HW-SW (hardware-software) contract



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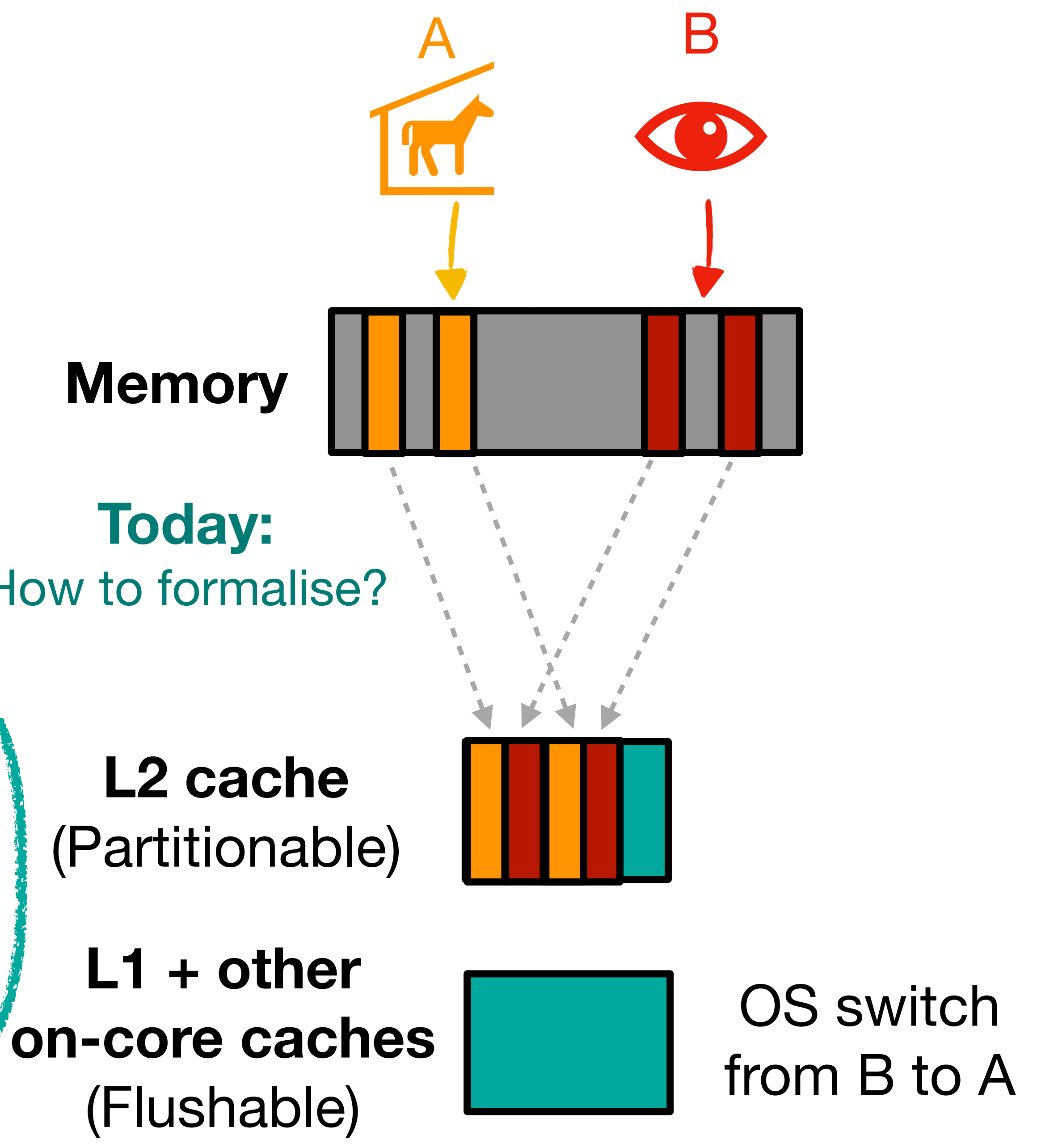

Today:
How to formalise?

"Flush": Write fixed content; wait up to fixed time.

How to formalise an OS enforces *time protection*?

Versus threat scenario:
trojan and spy

🐎 ➡ 👁

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No channels!

OS 🤝 HW

Abstract *covert state* + *time* to reflect strategies enabled by HW:
Partition or flush state; pad time.

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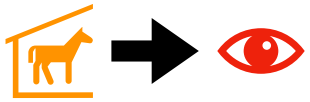

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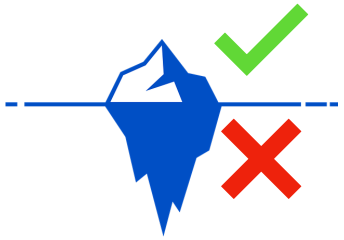

Make security property precise enough to exclude flows from covert state.

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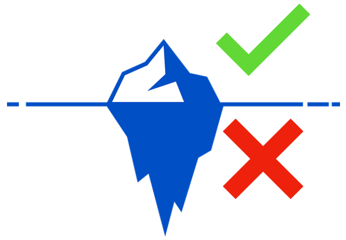

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Demonstrating these principles,
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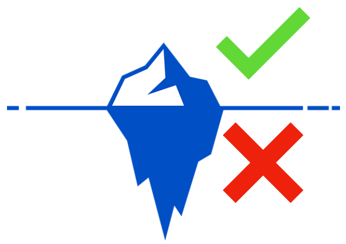

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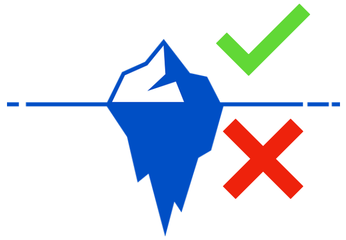

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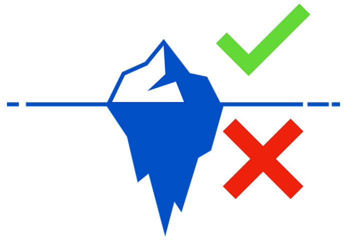

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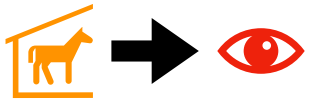

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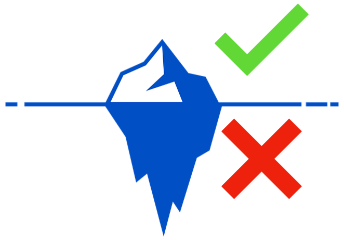

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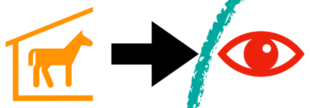

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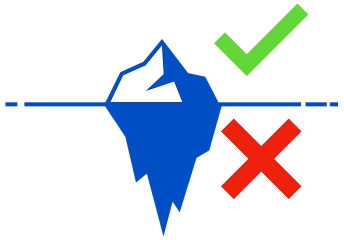

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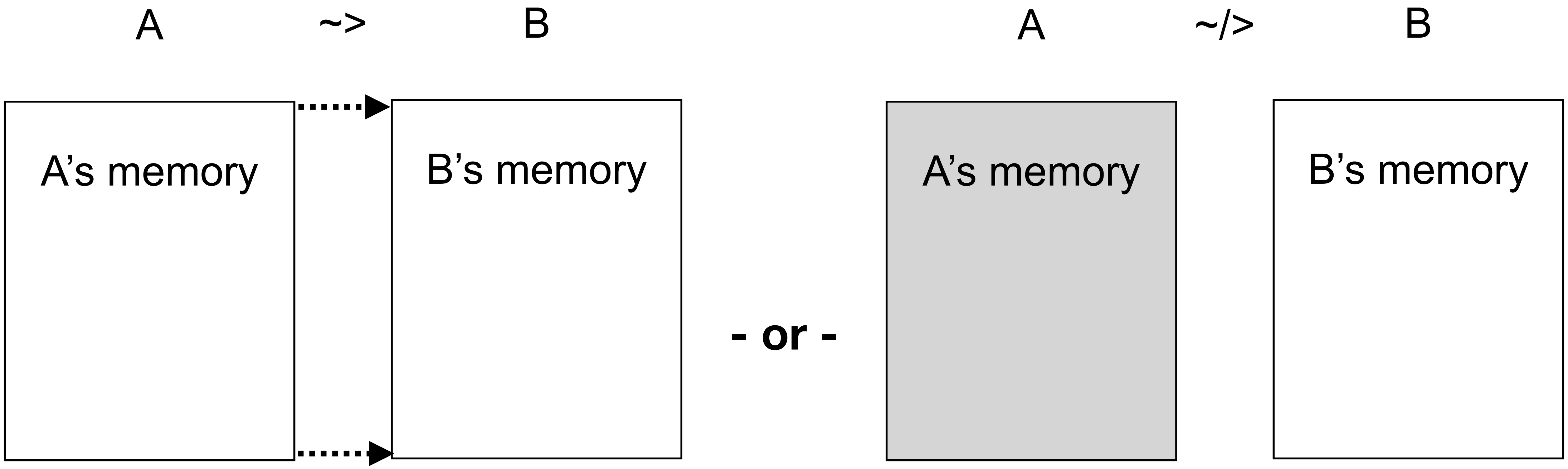
Overt vs *covert* state



A ~> B

A's memory

B's memory

- or -

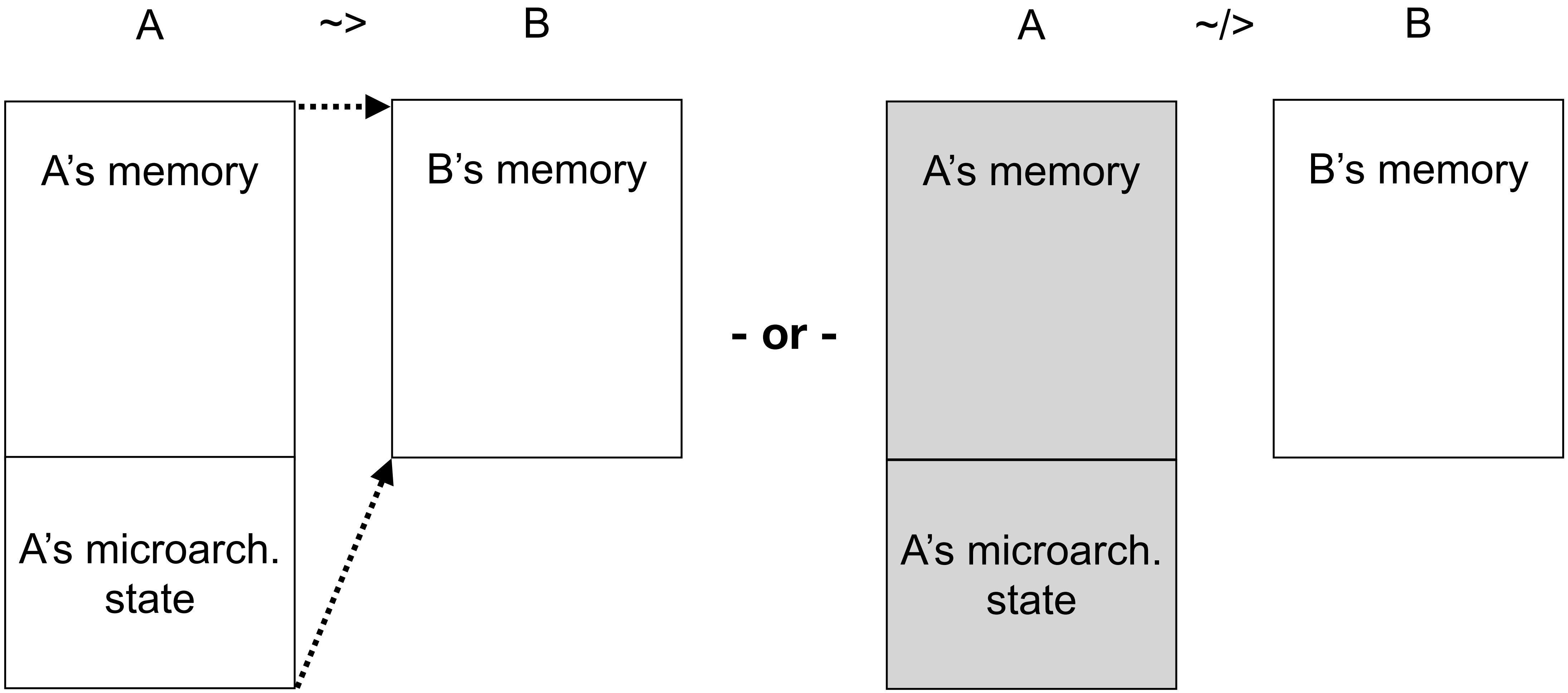
A ~/> B

A's memory

B's memory

From prior seL4 infoflow proofs
[Murray et al. 2012, 2013]:
"all or nothing" policies

Overt vs *covert* state



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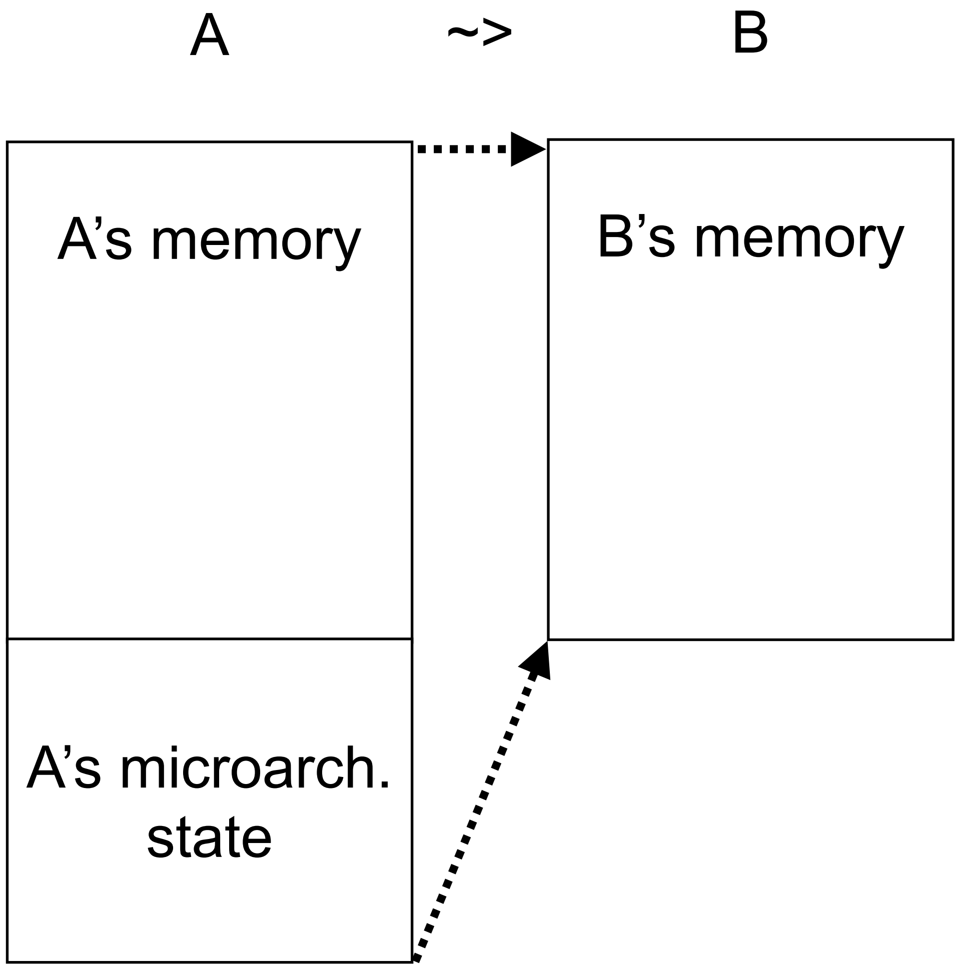
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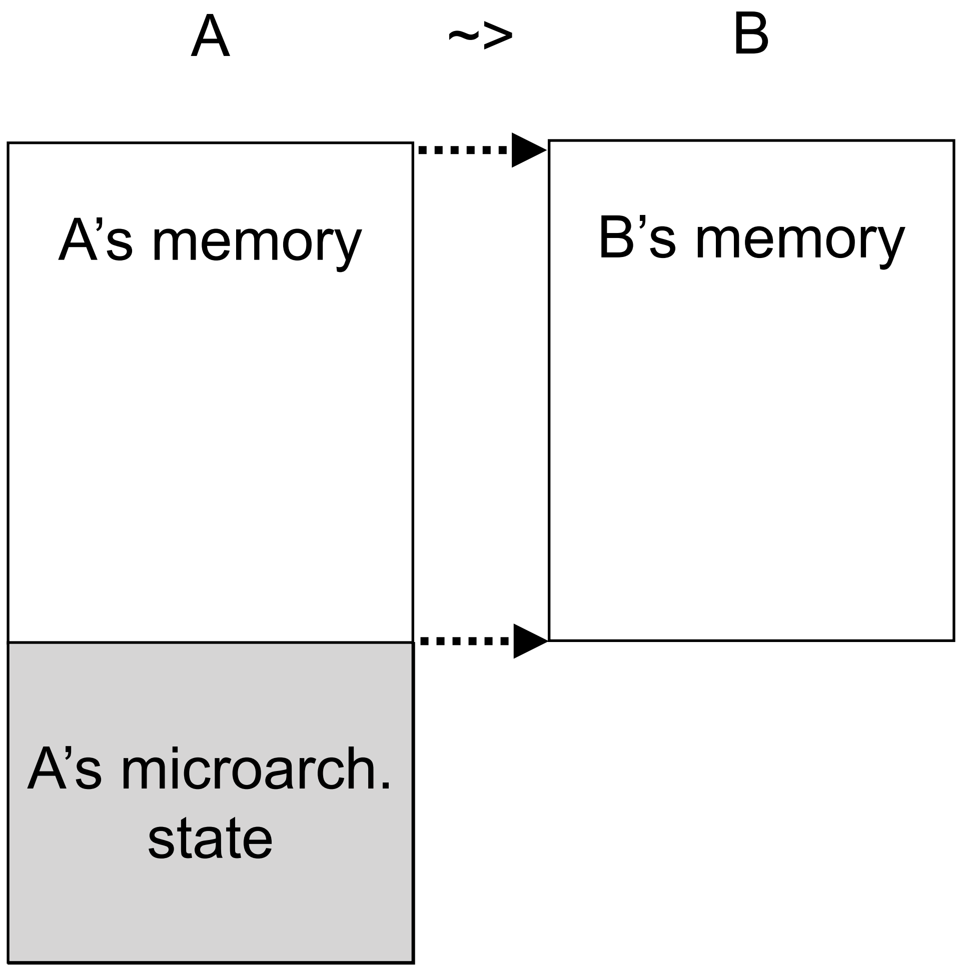
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A's memory

B's memory

A's microarch. state

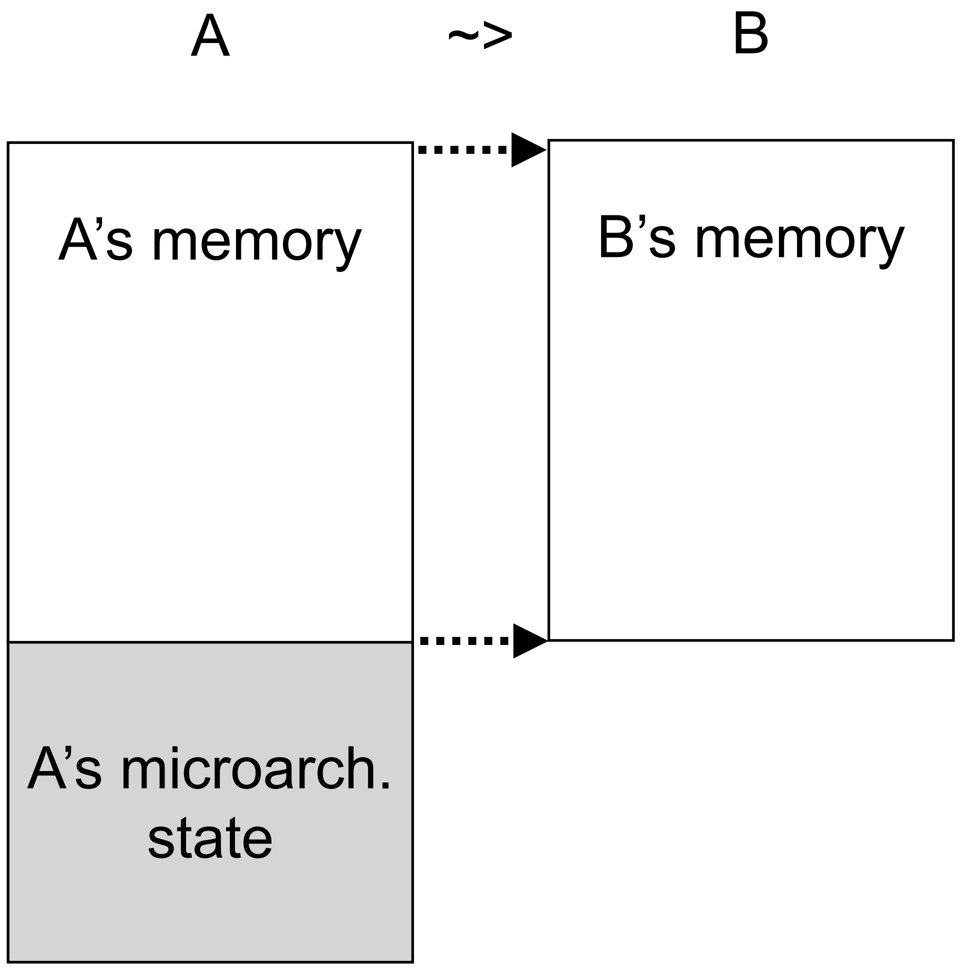
**Principle: Need policies
to allow some (*overt*) flows
while excluding other (*covert*) ones**

Covert state: Partitionable vs flushable

No channels!

OS 🤝 HW

<u>Principle</u>:
Model channels as *state elements*
by their *elimination strategy*
as per *HW-SW contract*



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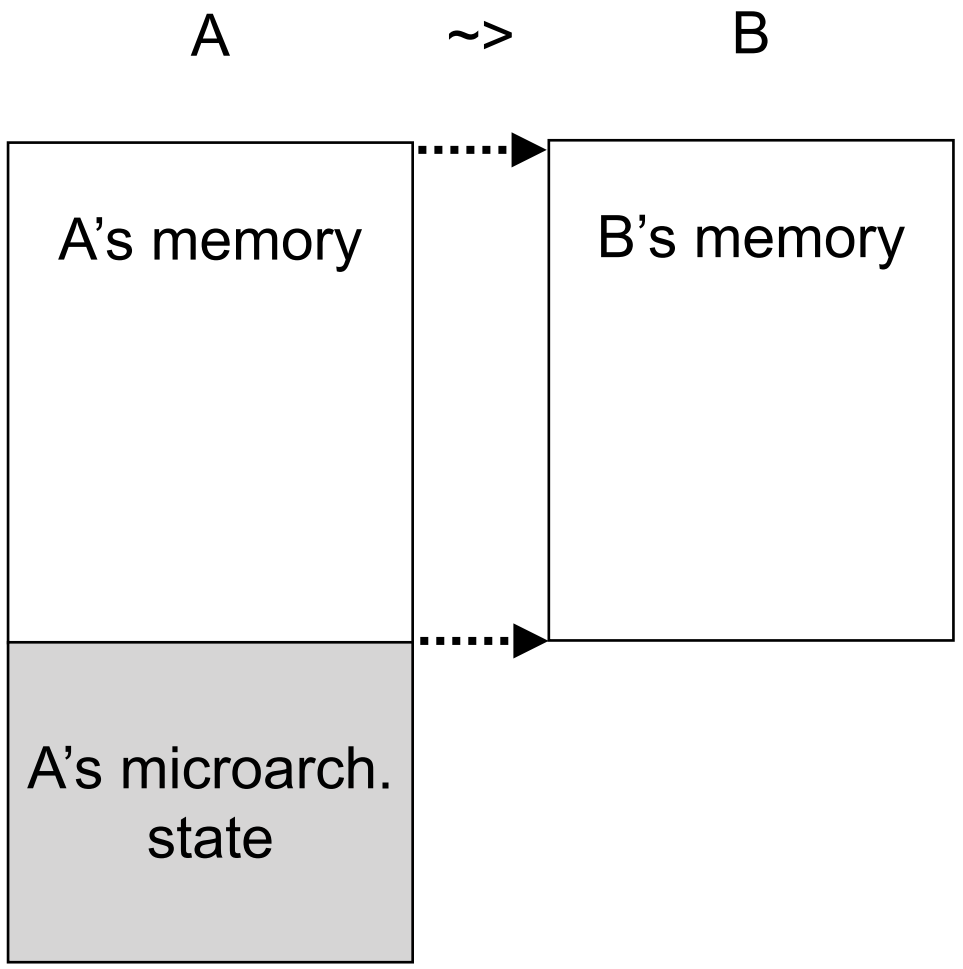

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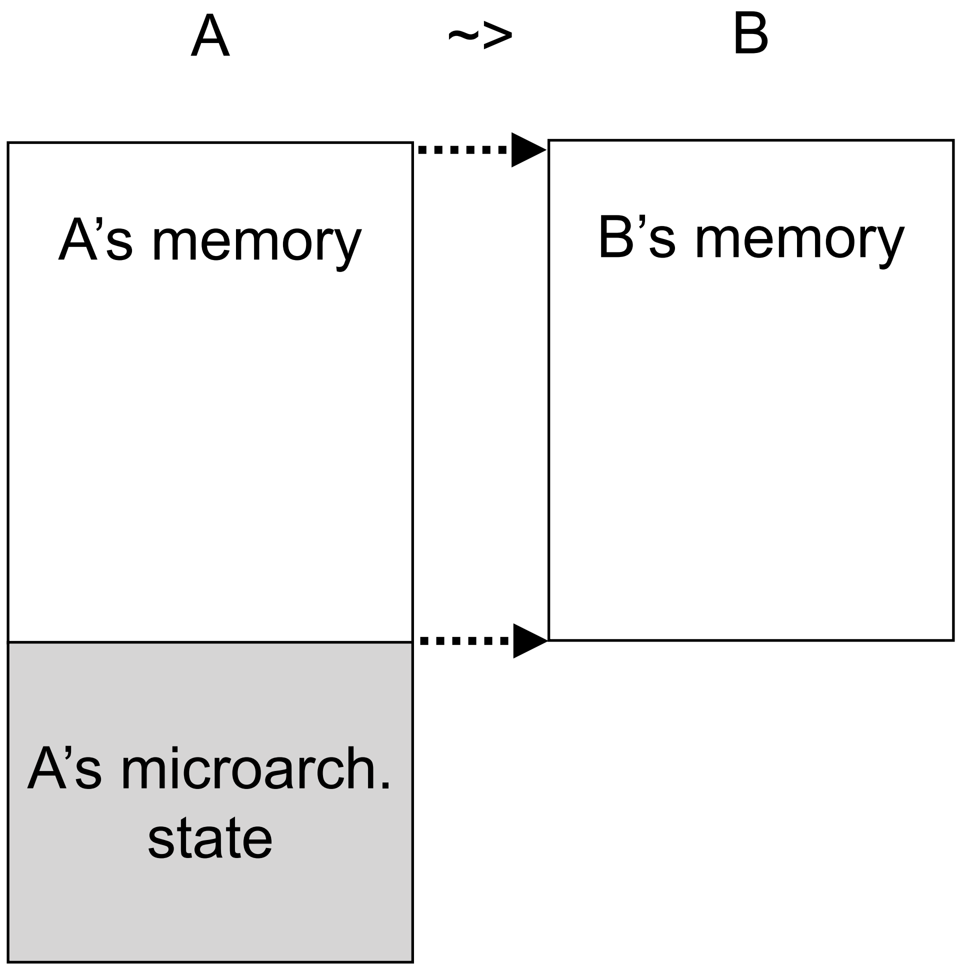

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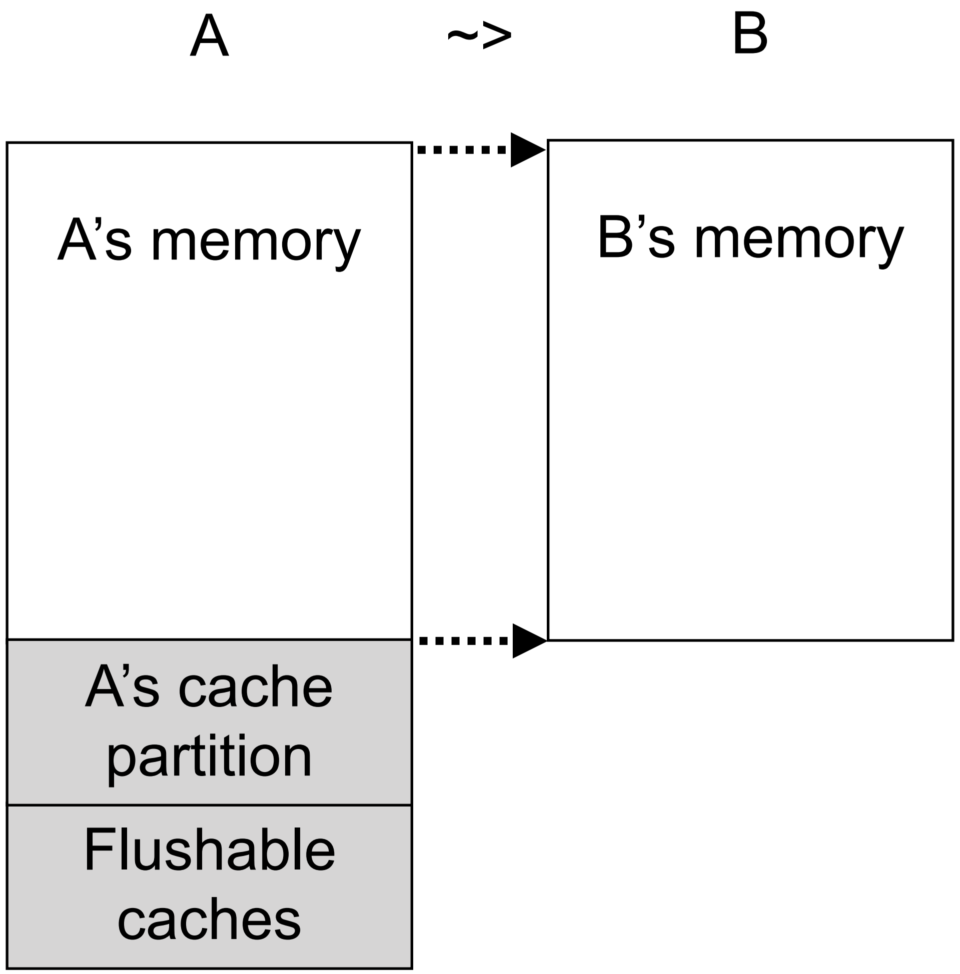

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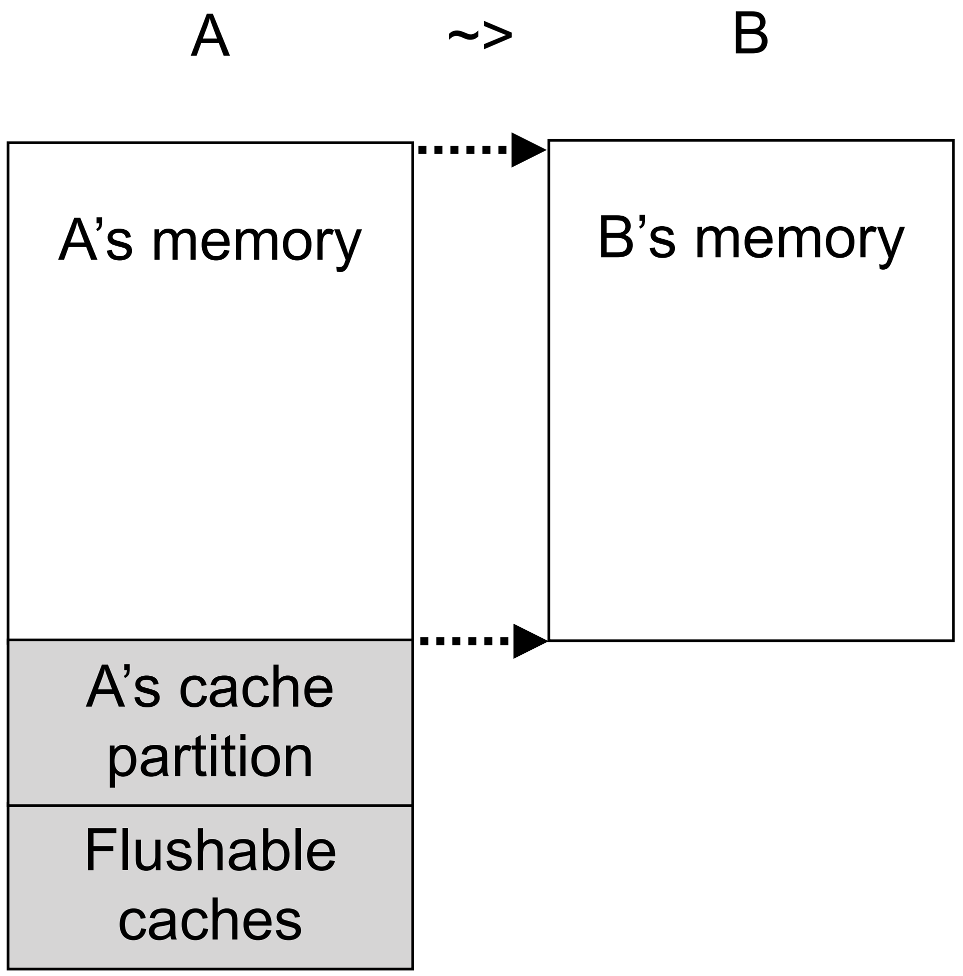

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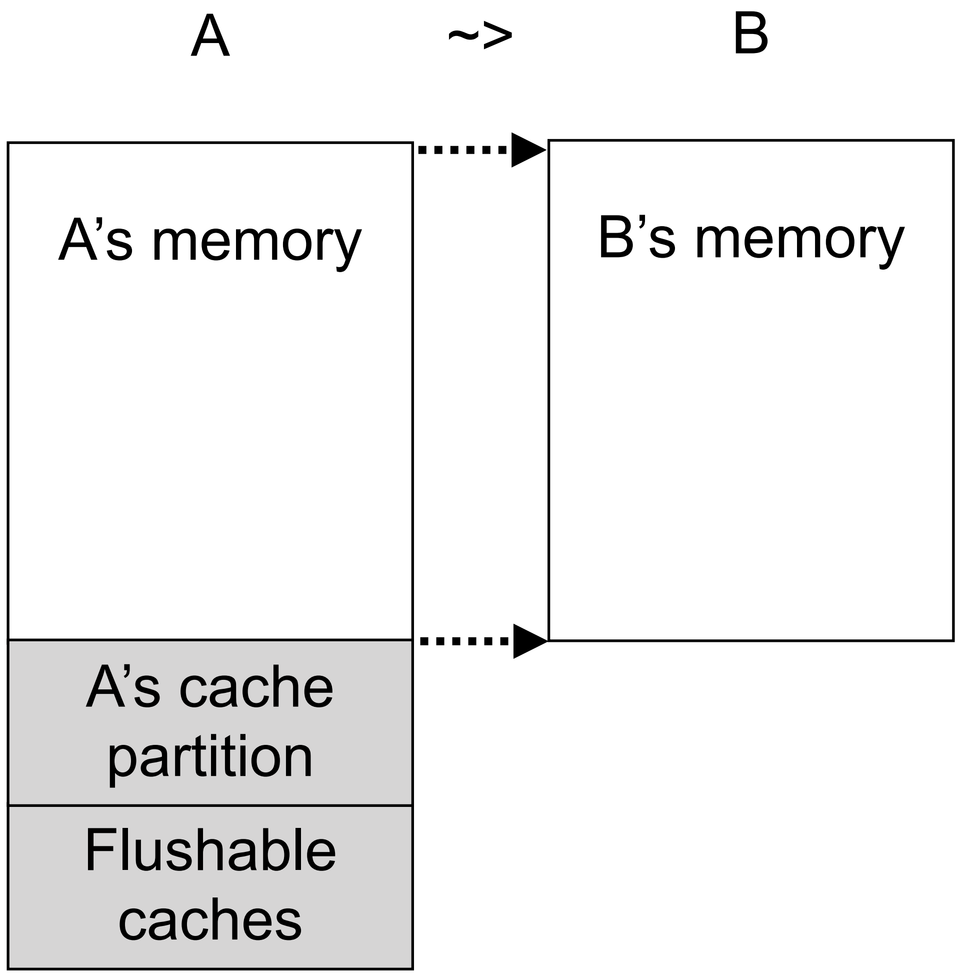
    - Interrupt-generating devices (partitionable; not pictured).



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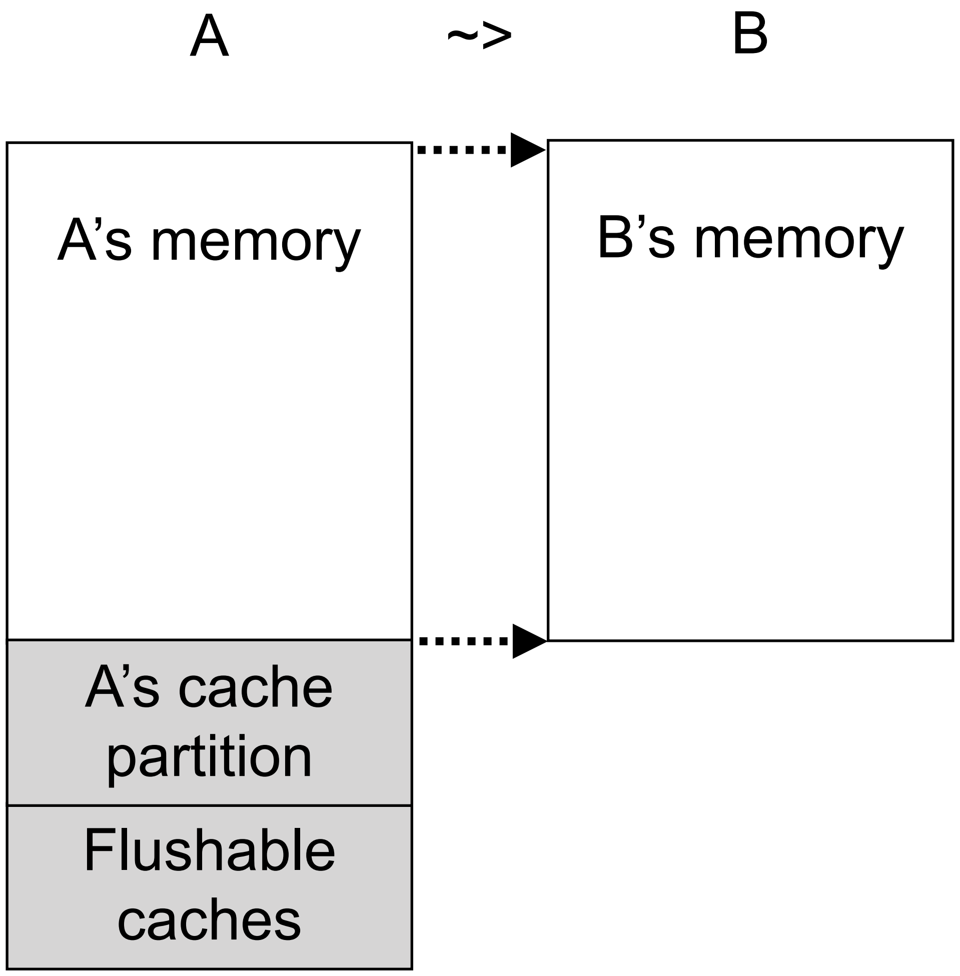
No channels!

OS 🤝 HW

<u>Principle</u>:
Model channels as *state elements*
by their *elimination strategy*
as per *HW-SW contract*

- Strategy for OS:
  Partition or *flush* state; *pad* time.
- Relies on HW-SW contract:
  - <u>State</u>: Everything must be *partitionable* or *flushable*.
    - e.g. Off-core vs on-core caches.
    - Interrupt-generating devices (partitionable; not pictured).
  - <u>Time</u>: HW must give reliable
    - WCETs (worst-case execution times)



A ~> B

A's memory

B's memory

A's cache partition

Flushable caches

Covert state: Partitionable vs flushable

No channels!

OS 🤝 HW

Principle:
Model channels as *state elements* by their *elimination strategy* as per *HW-SW contract*

- Strategy for OS:
  Partition or *flush* state; *pad* time.
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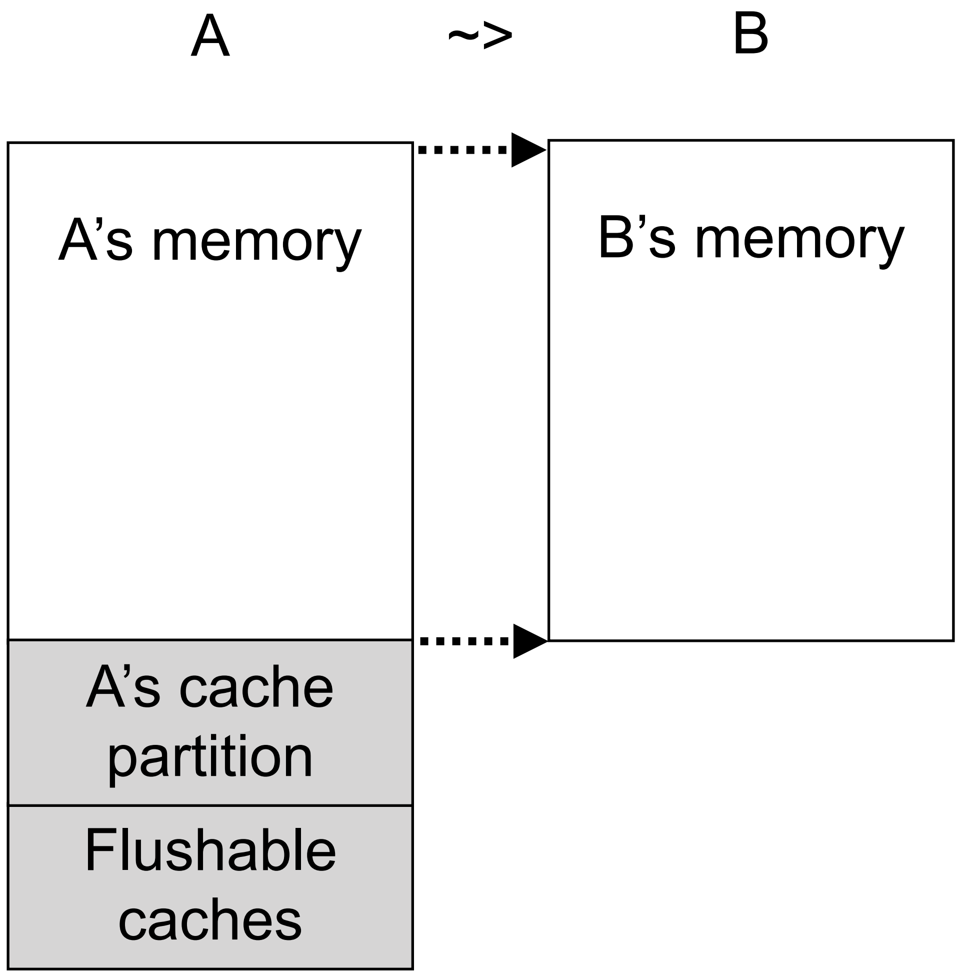
  - Time: HW must give reliable
    - WCETs (worst-case execution times)
    - method of *padding*.



How to formalise an OS enforces *time protection*?

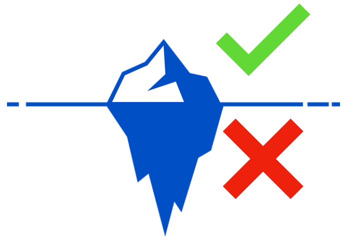
Versus threat scenario:
trojan and spy

🐴 ➡ 👁

No channels!

OS 🤝 HW

Abstract *covert state* + *time* to reflect strategies enabled by HW: Partition or flush state; pad time.



Make security property precise enough to exclude flows from covert state.

Demonstrating these principles, we formalised in Isabelle/HOL:

1. OS security model imposing requirements on relevant parts of OS.
(Intended for seL4, but *generic*)

2. OS security property that is dynamic; this makes it observer relative.
(Improving on seL4's of [Murray et al. 2012])

3. Proof our security property holds if OS model's requirements hold.

4. Basic instantiation of OS model exercising dynamic policy.

How to formalise an OS enforces *time protection*?

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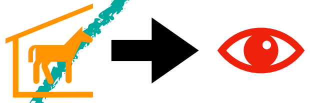
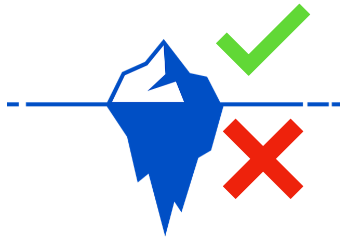


No channels!

OS 🤝 HW

Abstract *covert state* + *time* to reflect strategies enabled by HW: Partition or flush state; pad time.



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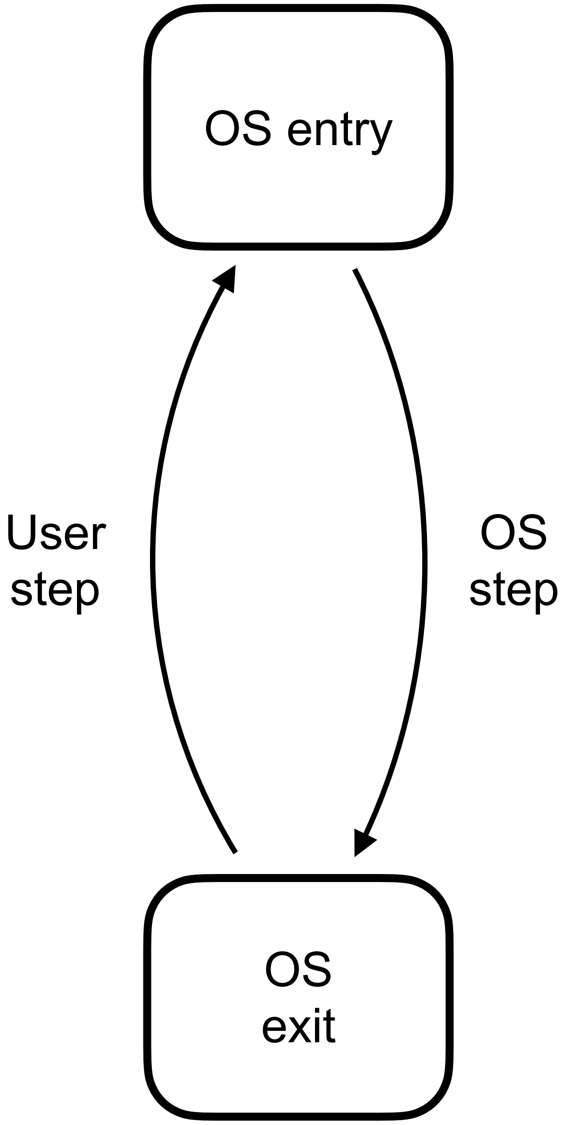
OS security model

Transition system

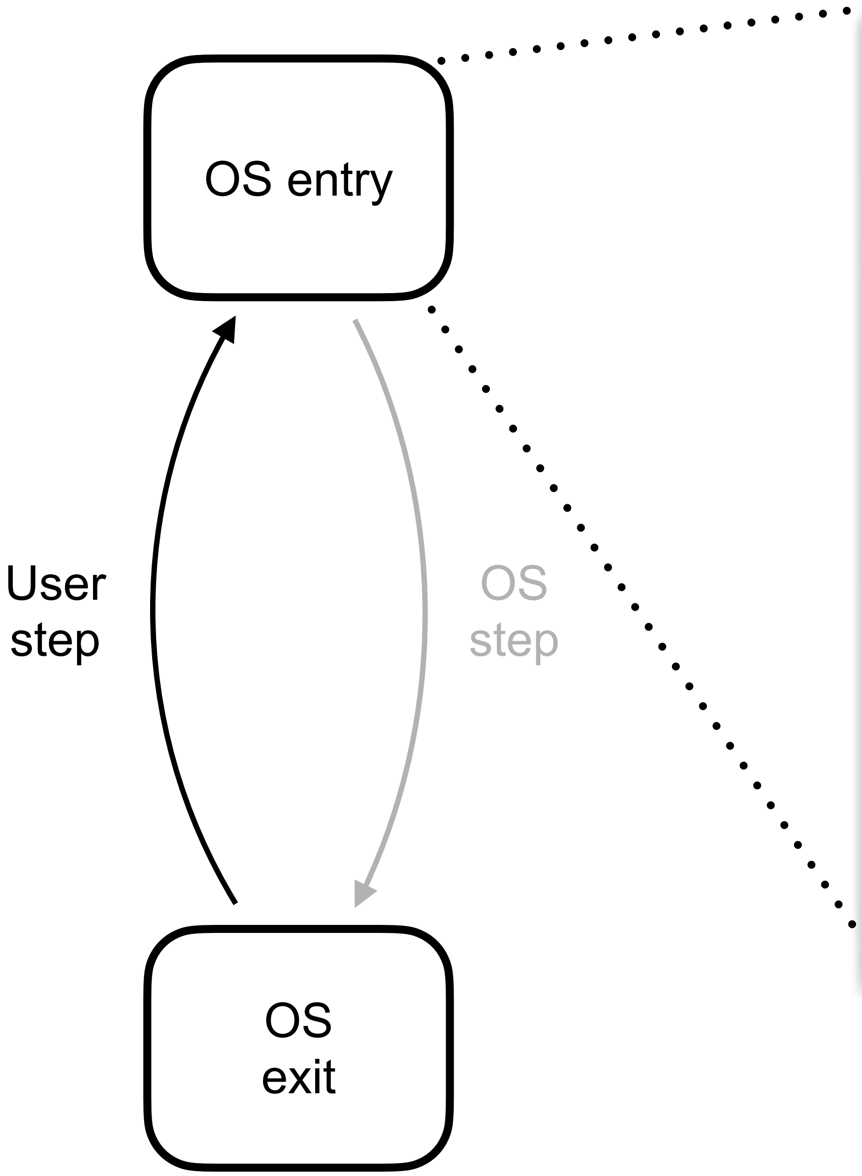


OS security model

No channels!

OS 🤝 HW

Transition system



State fields

mem :: *addr* ⇒ *int*

flst :: *addr* ⇒ bool /* Flushable microarch. */

pst :: *addr* ⇒ bool /* Partitionable microarch. */

tm :: *nat* /* Time */

dom :: *domain* /* Current domain */

devs :: *device* set /* Interrupt-generating devices */

event :: {Syscall, UserInterrupt, TimerInterrupt}

args :: *args* /* System call arguments */

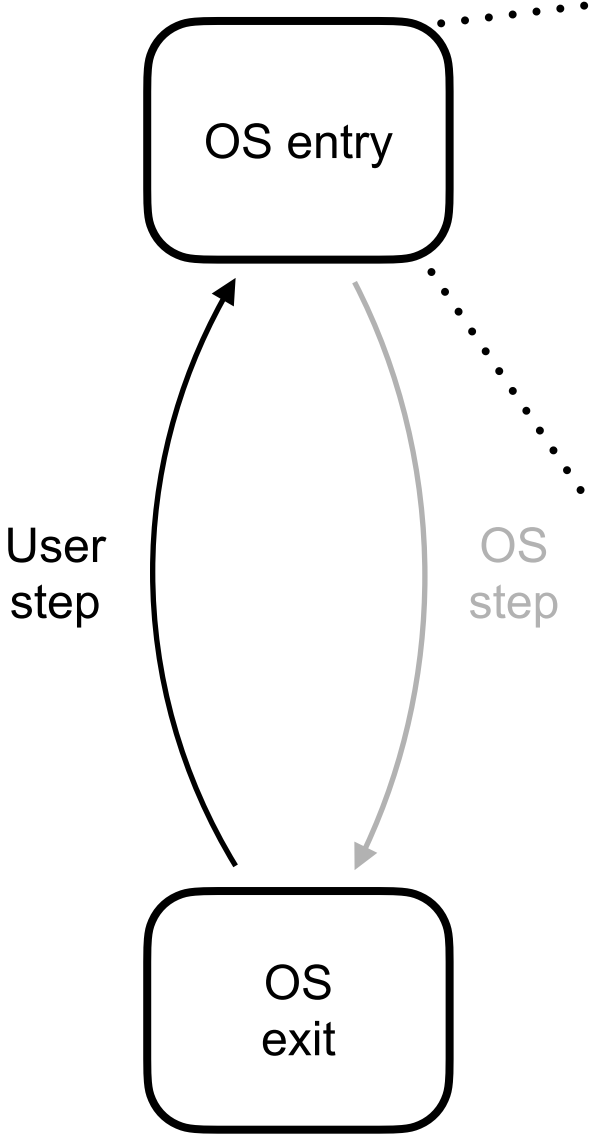
prot :: *prot* /* Protection state */

OS security model

No channels!

OS 🤝 HW

Transition system



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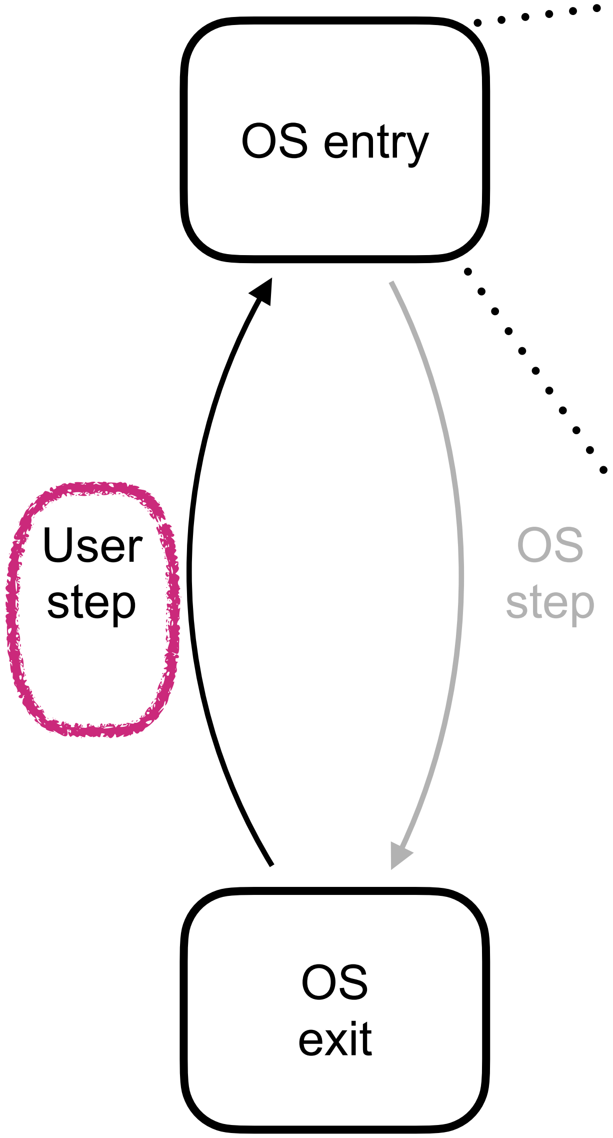
Microarchitecture
Devices

OS security model

No channels!

OS 🤝 HW

Transition system



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Microarchitecture

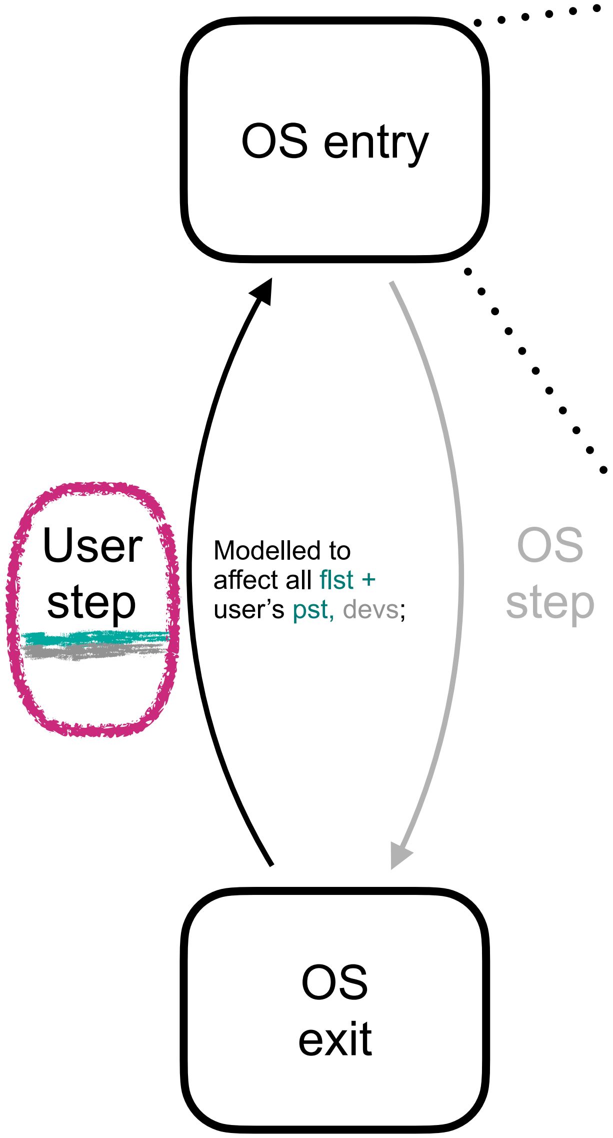
Devices

OS security model

No channels!

OS 🤝 HW

Transition system



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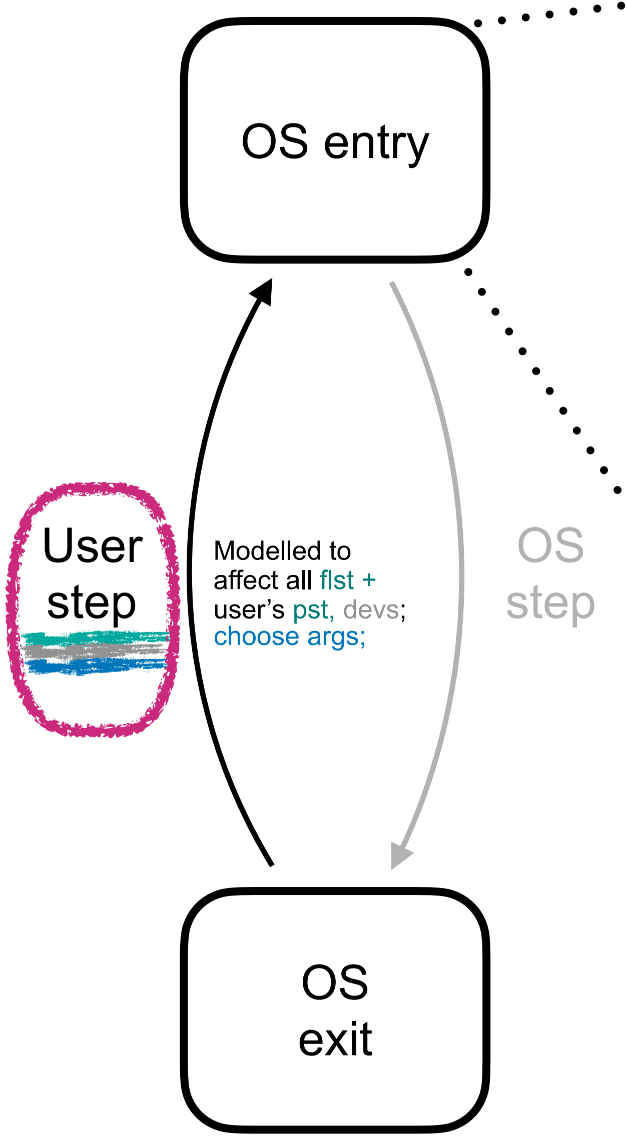
Microarchitecture
Devices

OS security model

No channels!

OS 🤝 HW

Transition system



OS entry
User step
Modelled to affect all flst + user's pst, devs; choose args;
OS step
OS exit

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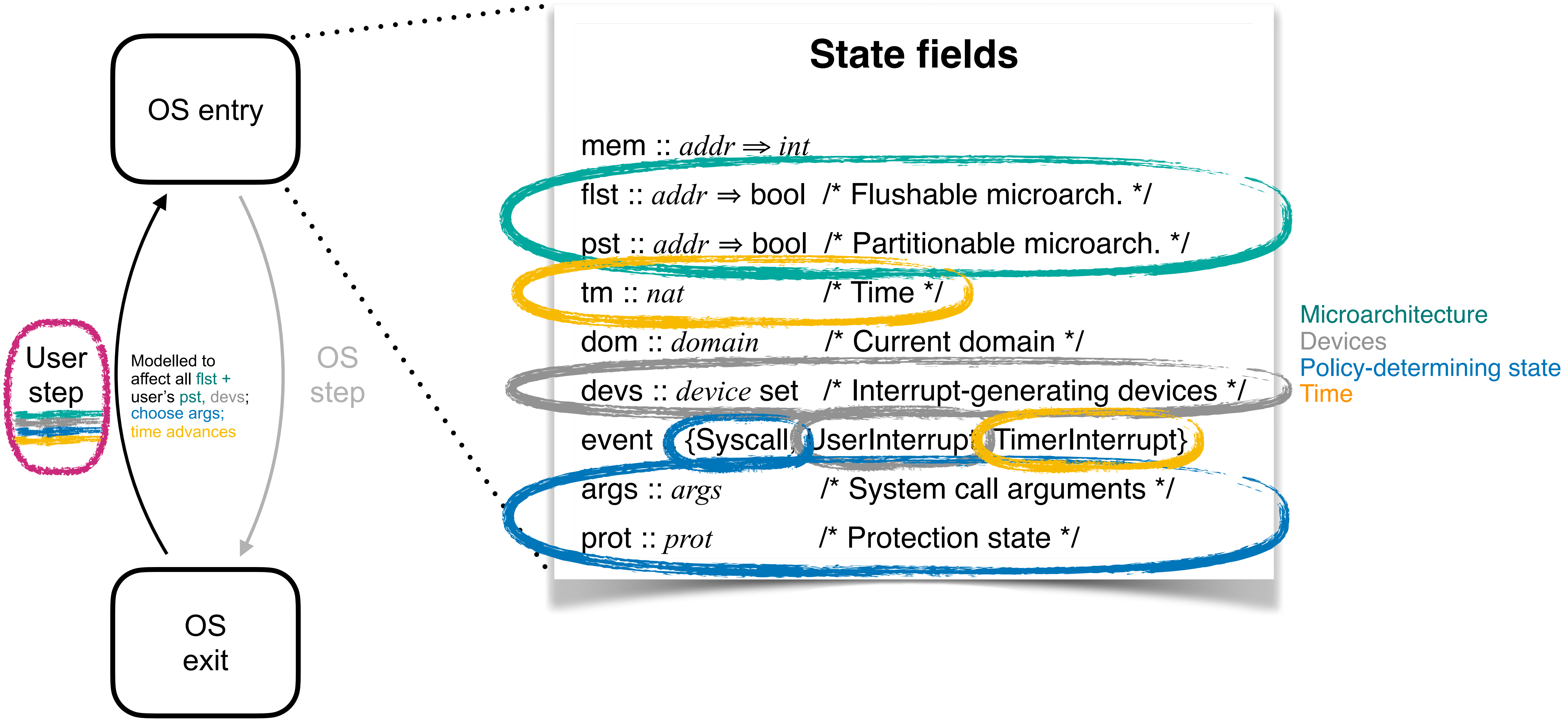
Microarchitecture
Devices
Policy-determining state

OS security model

No channels!

OS 🤝 HW

Transition system



OS entry
User step
Modelled to affect all flst + user's pst, devs; choose args; time advances
OS step
OS exit

State fields

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Microarchitecture
Devices
Policy-determining state
Time

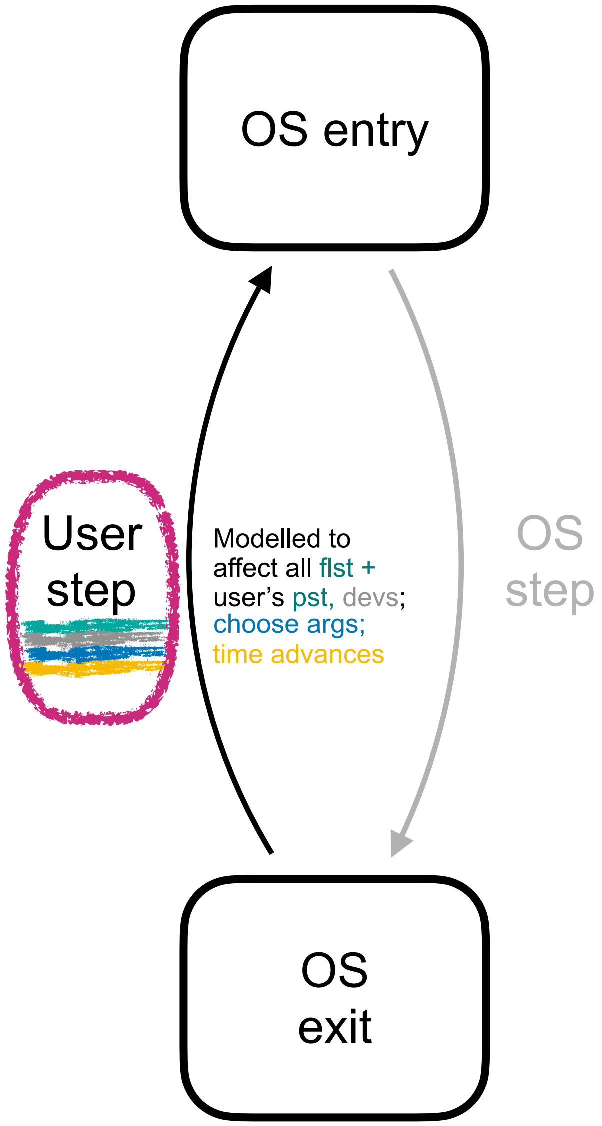
OS security model

No channels!

OS 🤝 HW

Microarchitecture
Devices
Policy-determining state
Time

Transition system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OS security model

No channels!

OS 🤝 HW

Microarchitecture
Devices
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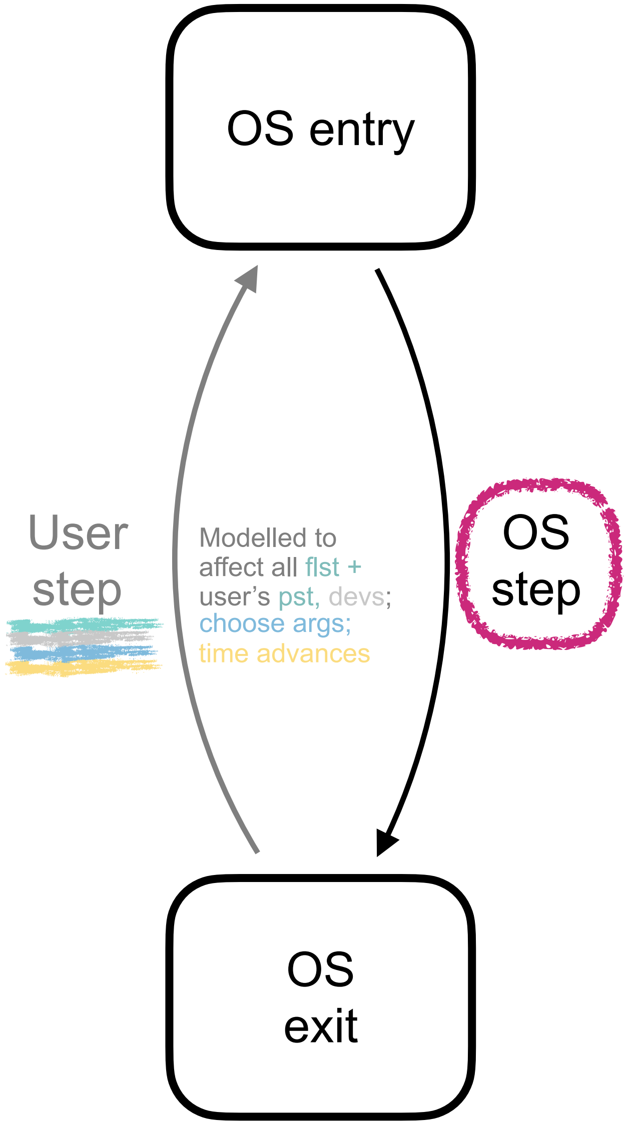
Time

Transition system



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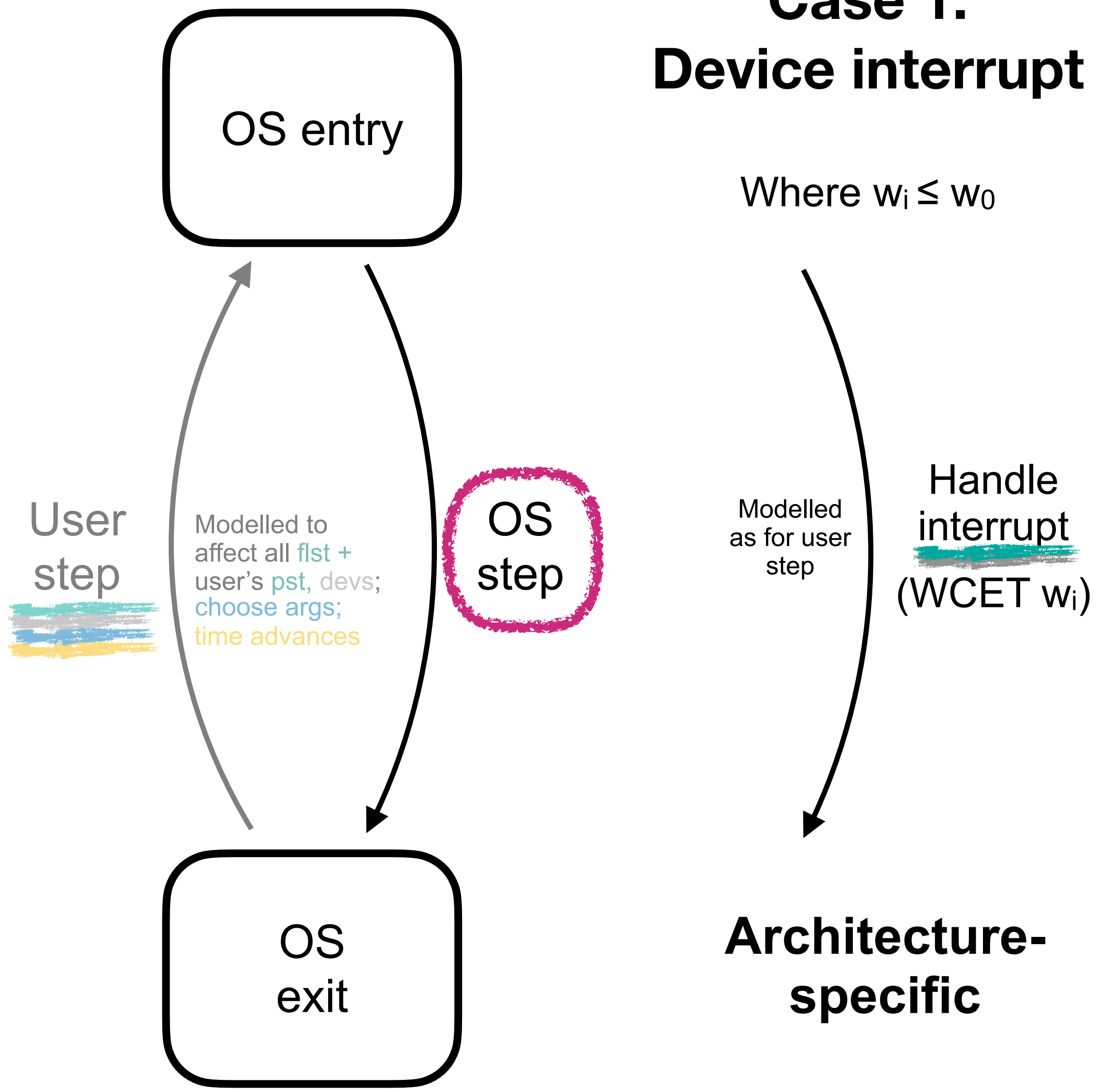
OS security model

No channels!

OS 🤝 HW

Microarchitecture
Devices
Policy-determining state
Time

Transition system



OS entry

OS exit

User step

Modelled to affect all flst + user's pst, devs; choose args; time advances

OS step

Case 1: Device interrupt

Where $w_i \leq w_0$

Modelled as for user step

Handle interrupt (WCET w_i)

Architecture-specific

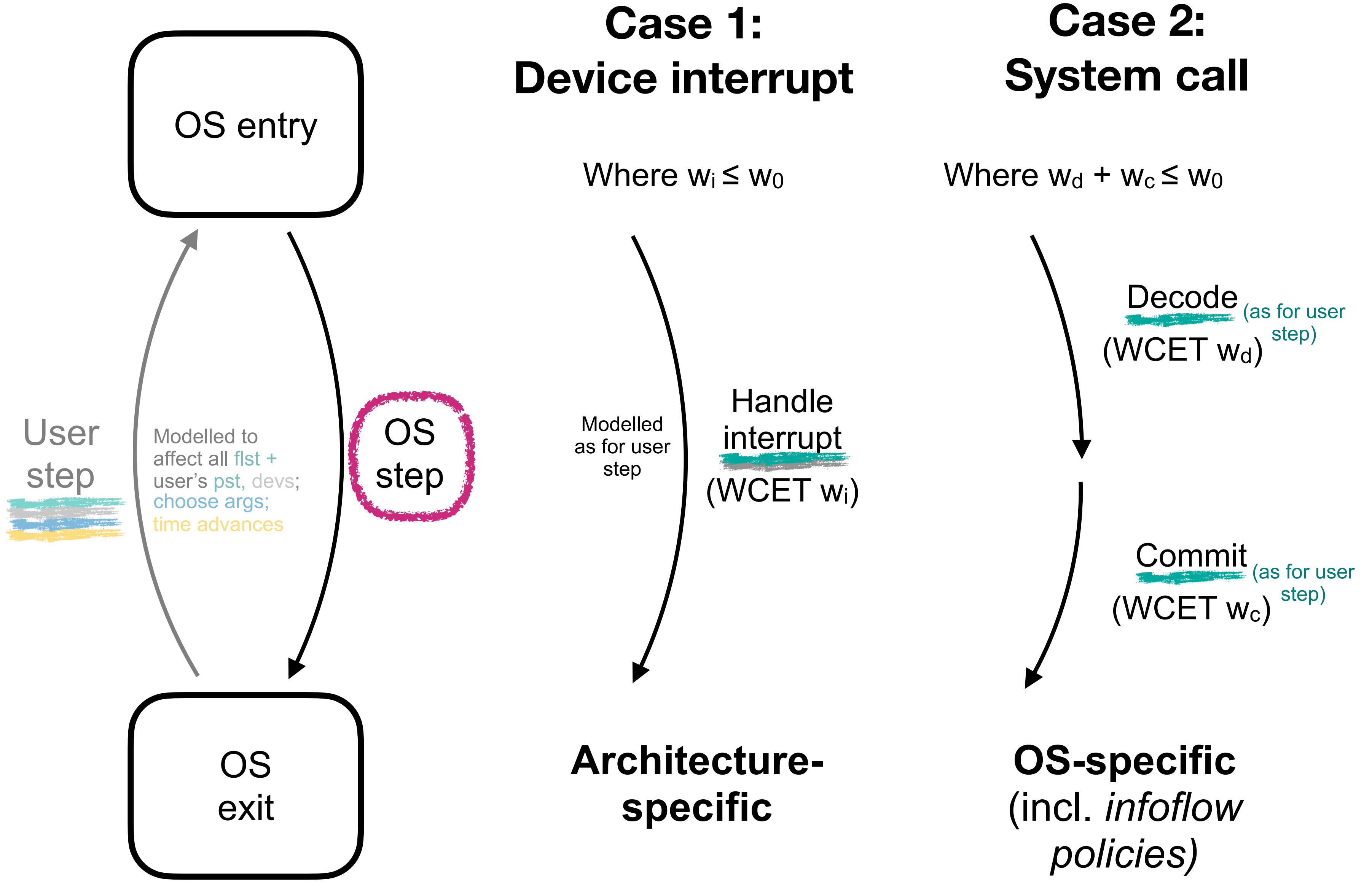
OS security model

No channels!

OS 🤝 HW

Microarchitecture
Devices
Policy-determining state
Time

Transition system



OS entry

User step

Modelled to affect all flst + user's pst, devs; choose args; time advances

OS step

OS exit

Case 1: Device interrupt

Where $w_i \leq w_0$

Modelled as for user step

Handle interrupt (WCET w_i)

Architecture-specific

Case 2: System call

Where $w_d + w_c \leq w_0$

Decode (as for user step) (WCET w_d)

Commit (as for user step) (WCET w_c)

OS-specific (incl. *infoflow policies)*

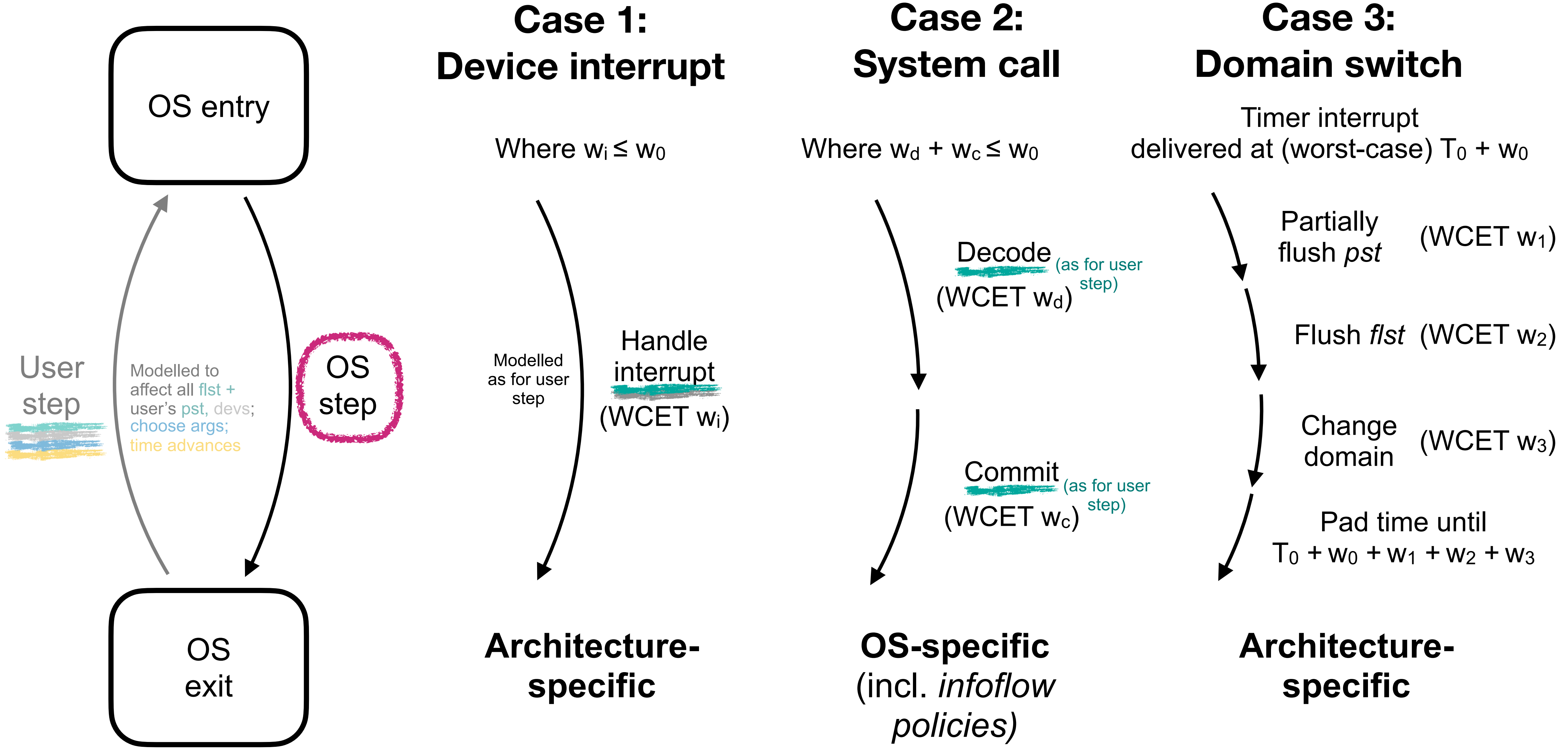
OS security model

No channels!

OS 🤝 HW

Microarchitecture
Devices
Policy-determining state
Time

Transition system



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OS-specific (incl. *infoflow policies*)

Case 3: Domain switch

Timer interrupt delivered at (worst-case) $T_0 + w_0$

Partially flush *pst* (WCET w_1)

Flush *flst* (WCET w_2)

Change domain (WCET w_3)

Pad time until $T_0 + w_0 + w_1 + w_2 + w_3$

Architecture-specific

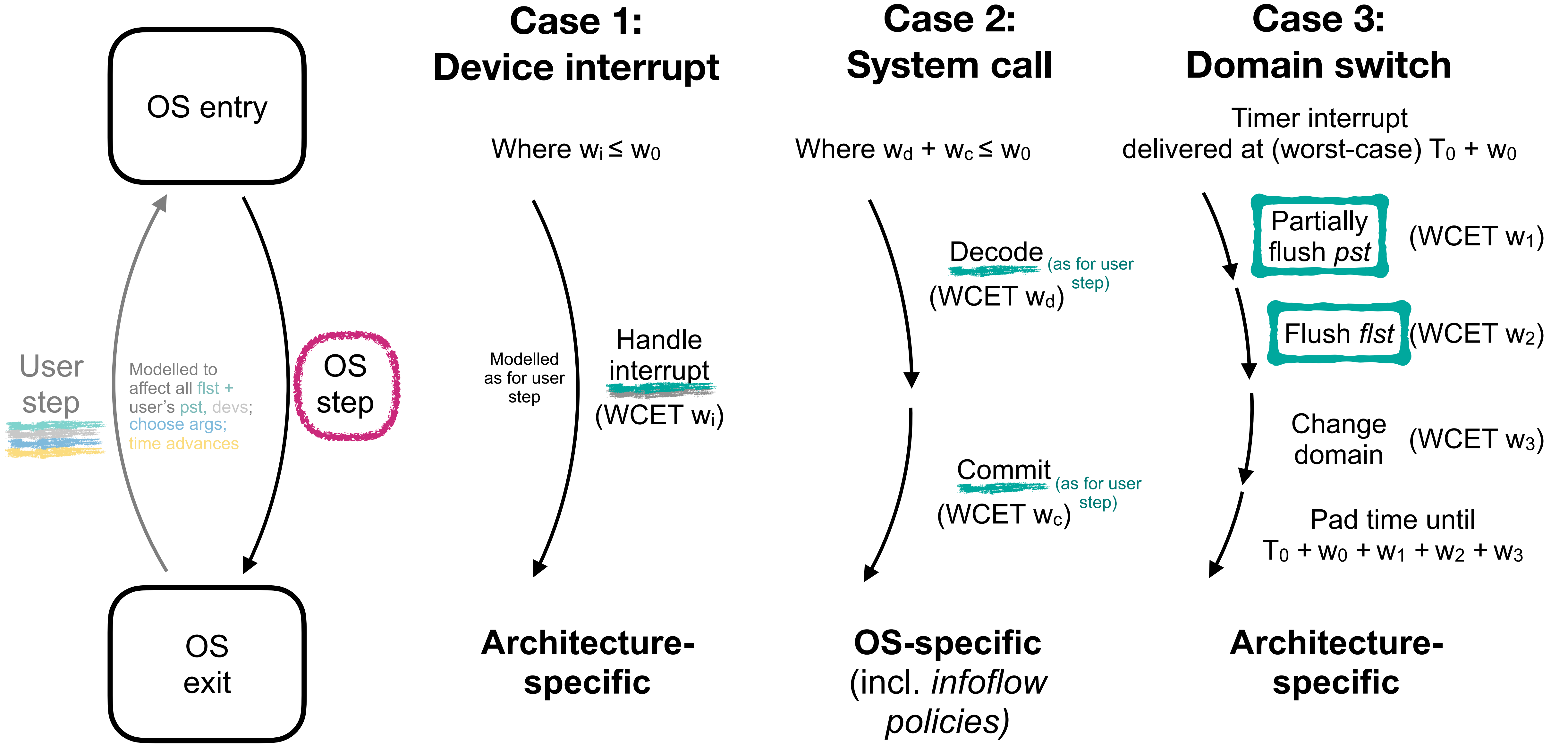
OS security model

No channels!

OS 🤝 HW

Microarchitecture
Devices
Policy-determining state
Time

Transition system



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OS 🤝 HW

Microarchitecture
Devices
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Time

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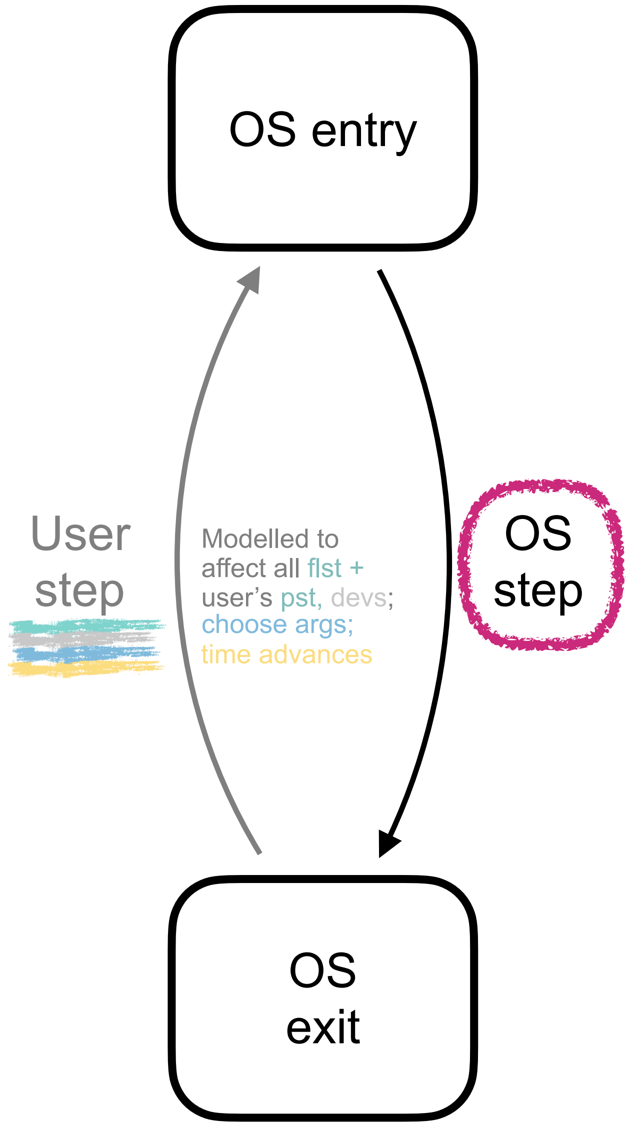

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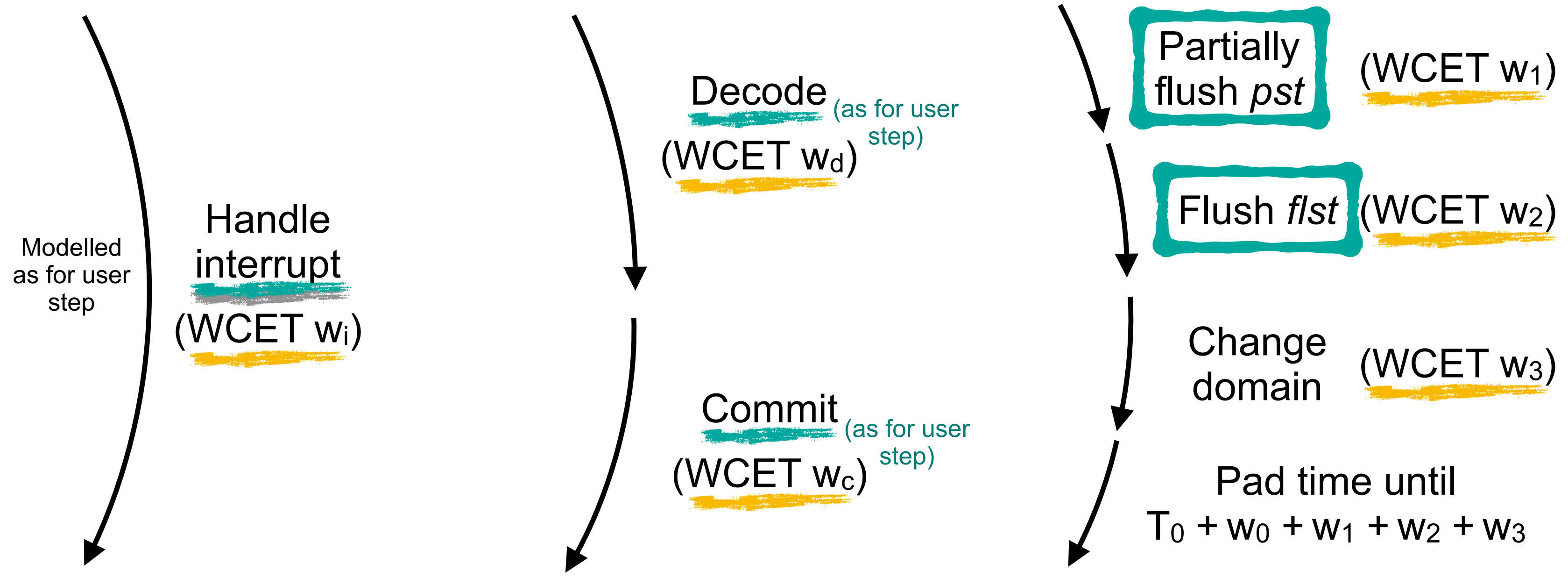

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Architecture-specific

OS-specific (incl. *infoflow policies)*

Architecture-specific

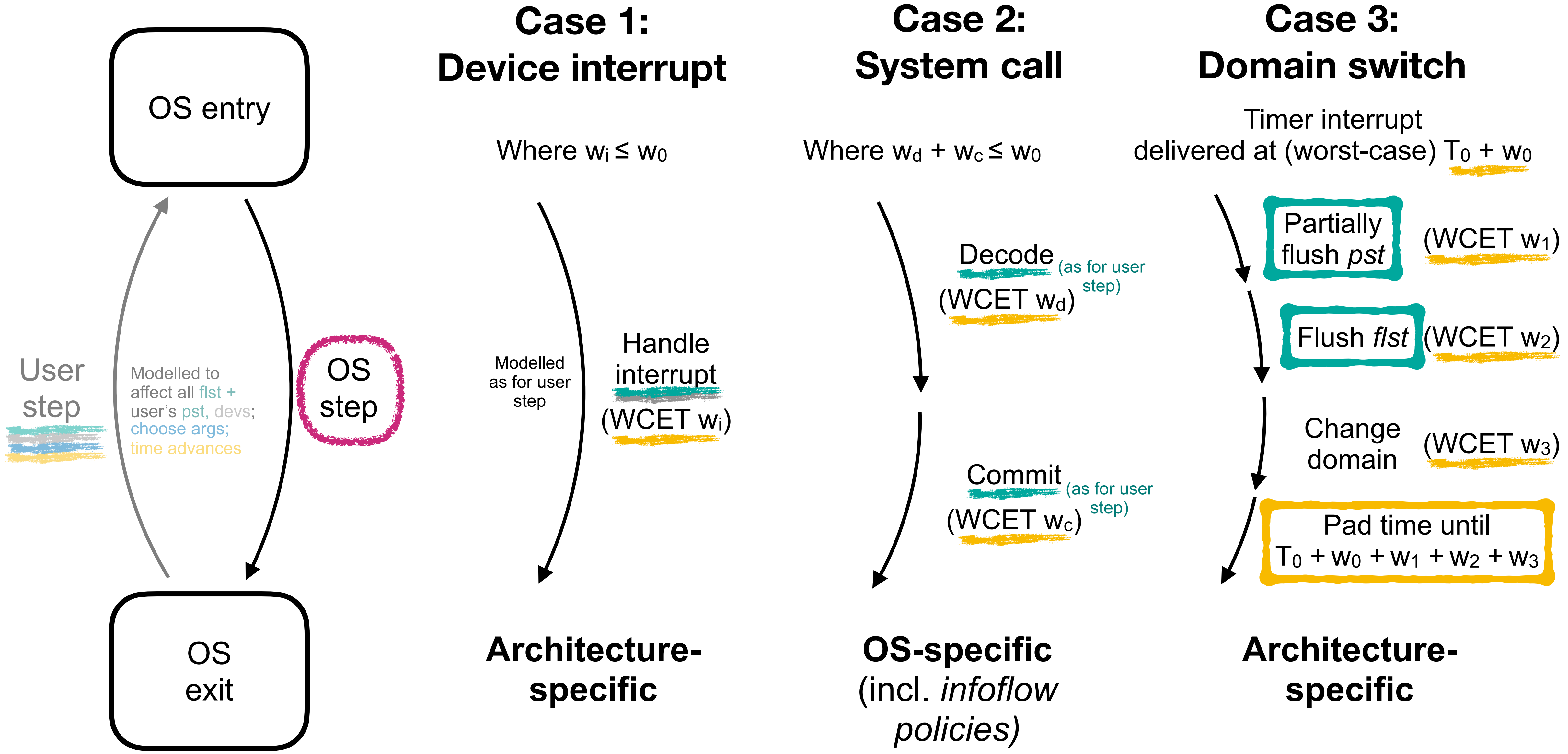
OS security model

No channels!

OS 🤝 HW

Microarchitecture
Devices
Policy-determining state
Time

Transition system



OS entry

OS exit

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(WCET w_c)

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Architecture-specific

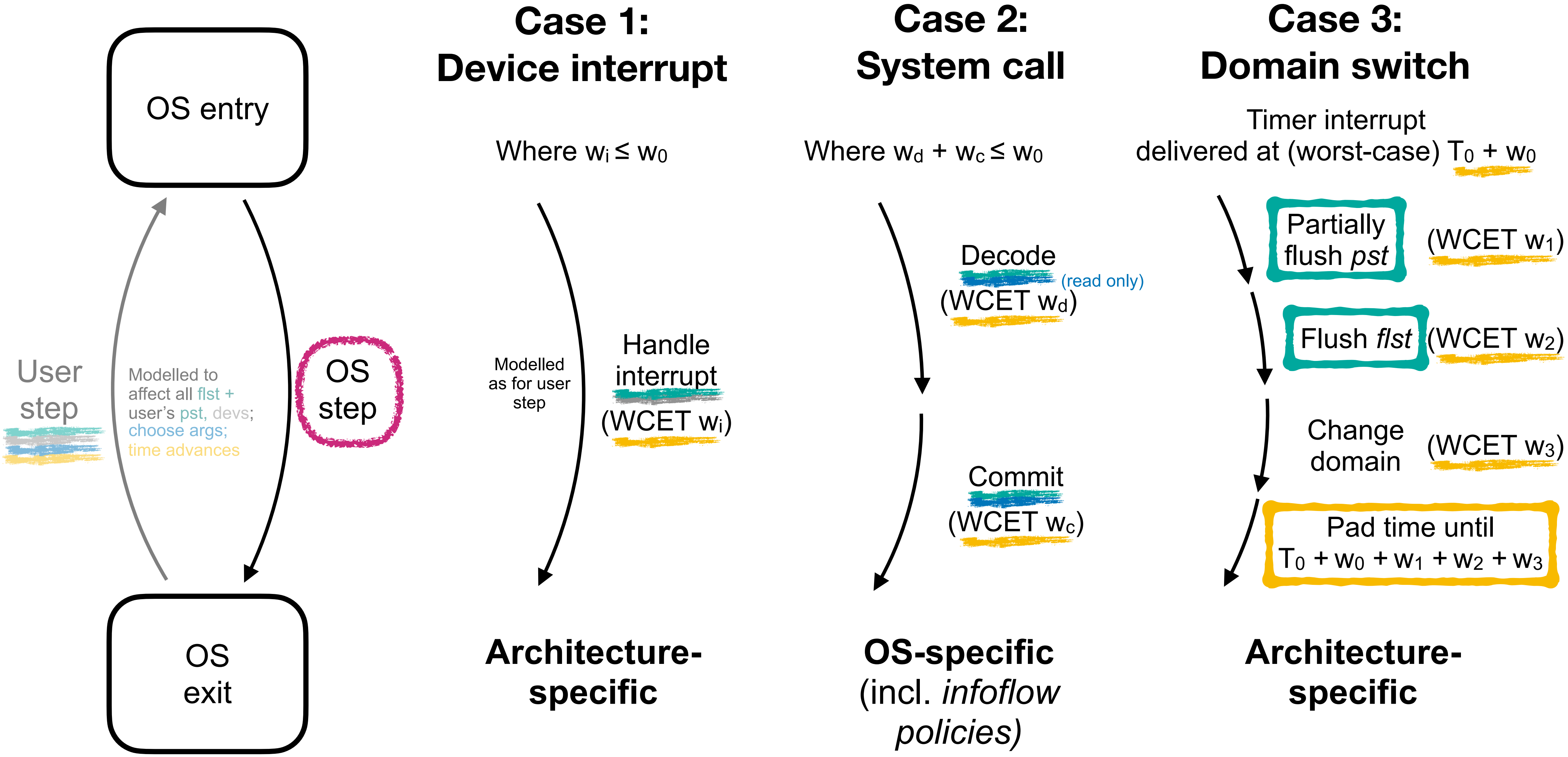
OS security model

No channels!

OS 🤝 HW

Microarchitecture
Devices
Policy-determining state
Time

Transition system



OS entry

User step

Modelled to affect all *flst* + user's *pst*, devs; choose args; time advances

OS step

OS exit

Case 1: Device interrupt

Where $w_i \leq w_0$

Modelled as for user step

Handle interrupt ($\mathrm{WCET}\ w_i$)

Architecture-specific

Case 2: System call

Where $w_d + w_c \leq w_0$

Decode ($\mathrm{WCET}\ w_d$) (read only)

Commit ($\mathrm{WCET}\ w_c$)

OS-specific (incl. *infoflow policies)*

Case 3: Domain switch

Timer interrupt delivered at (worst-case) $T_0 + w_0$

Partially flush *pst* ($\mathrm{WCET}\ w_1$)

Flush *flst* ($\mathrm{WCET}\ w_2$)

Change domain ($\mathrm{WCET}\ w_3$)

Pad time until $T_0 + w_0 + w_1 + w_2 + w_3$

Architecture-specific

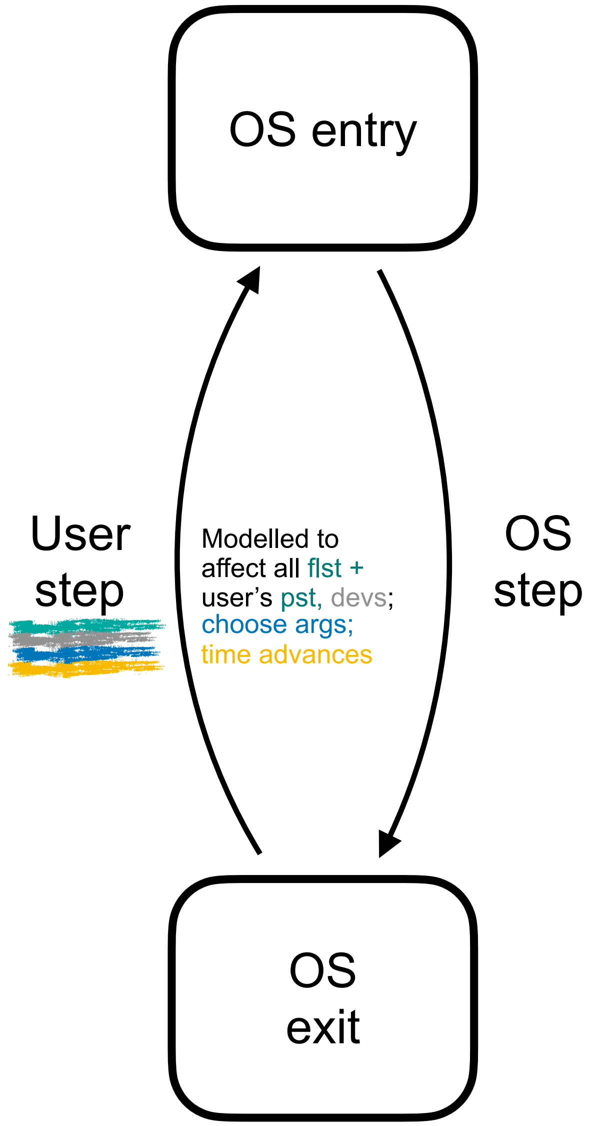
Security proof approach

No channels!

OS 🤝 HW

Microarchitecture
Devices
Policy-determining state
Time

Transition system



OS entry

User step

Modelled to affect all flst + user's pst, devs; choose args; time advances

OS step

OS exit

Case 1: Device interrupt

Case 2: System call

Case 3: Domain switch

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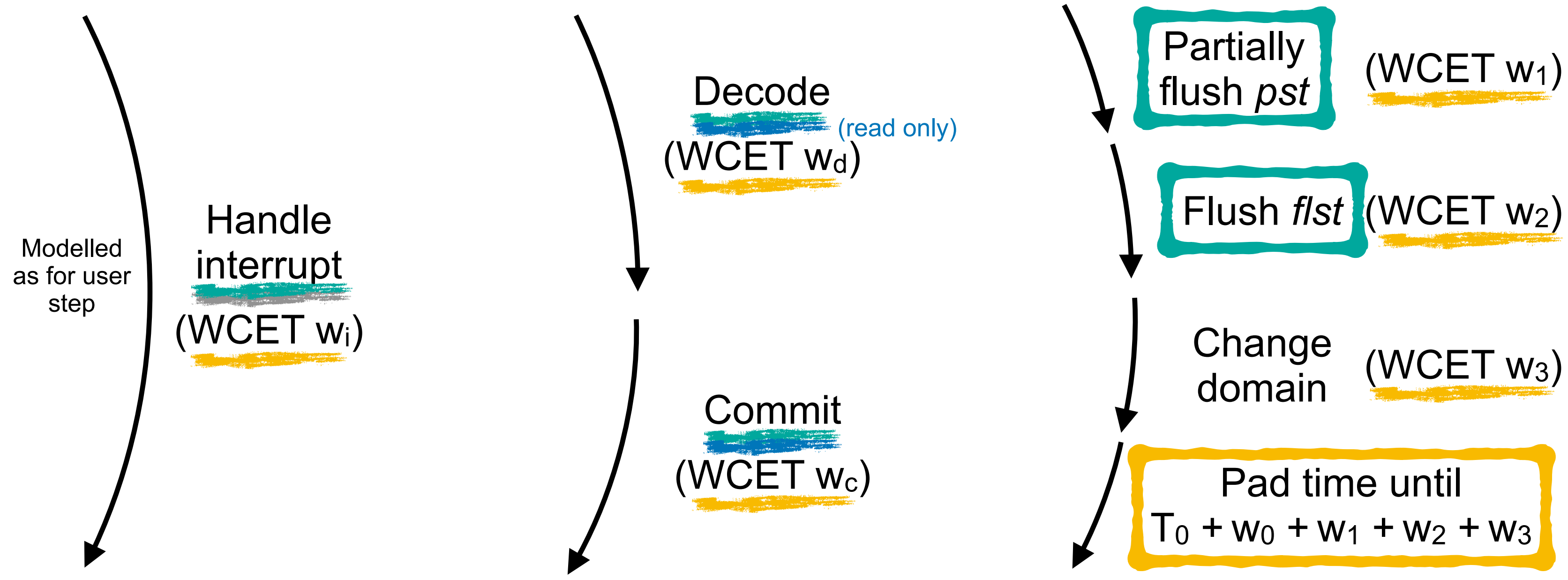

Modelled as for user step

Handle interrupt ($\text{WCET } w_i$)

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Change domain ($\text{WCET } w_3$)

Pad time until $T_0 + w_0 + w_1 + w_2 + w_3$

Architecture-specific

OS-specific (incl. *infoflow policies*)

Architecture-specific

Security proof approach

No channels!

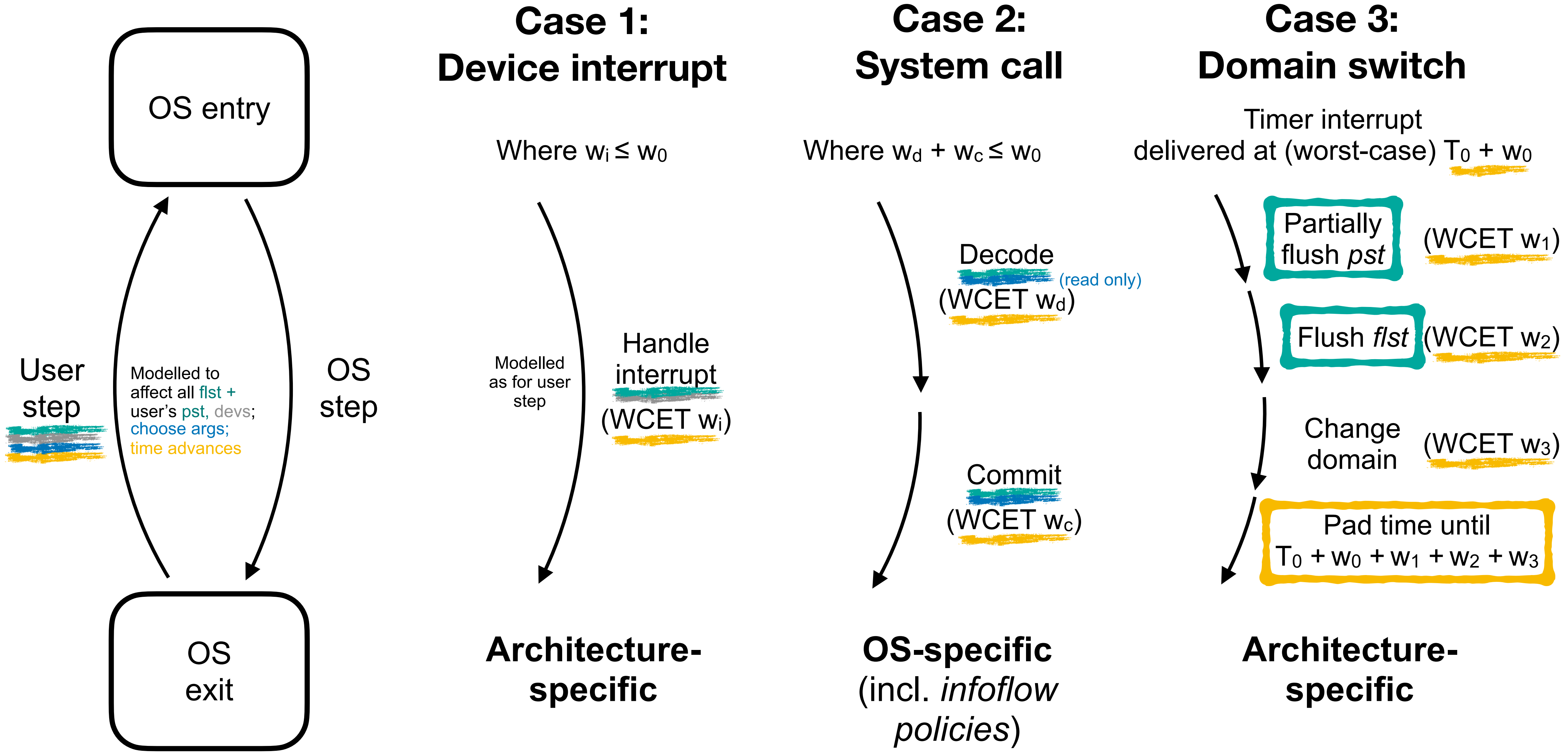
OS 🤝 HW

Requirements

(In addition to WCETs)

Microarchitecture
Devices
Policy-determining state
Time

Transition system



OS entry

User step

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OS step

OS exit

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Modelled as for user step

Handle interrupt (WCET w_i)

Architecture-specific

Case 2: System call

Where $w_d + w_c \leq w_0$

Decode (WCET w_d)

(read only)

Commit (WCET w_c)

OS-specific (incl. *infoflow policies*)

Case 3: Domain switch

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Architecture-specific

Security proof approach

No channels!

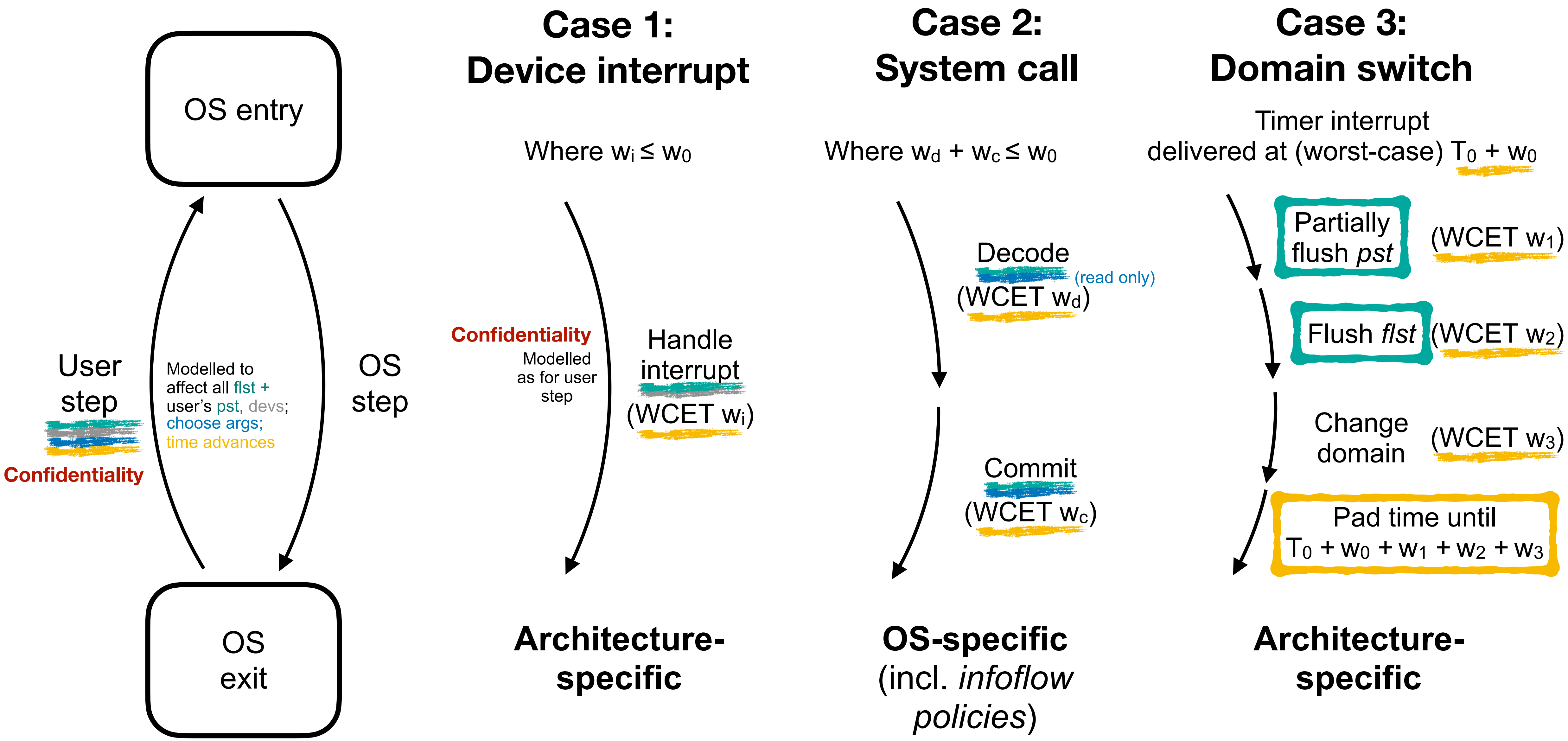
OS 🤝 HW

Microarchitecture
Devices
Policy-determining state
Time

Requirements

(In addition to WCETs)

Transition system



OS entry

User step

Modelled to affect all flst + user's pst, devs; choose args; time advances

Confidentiality

OS step

OS exit

Case 1: Device interrupt

Where $w_i \leq w_0$

Confidentiality

Modelled as for user step

Handle interrupt (WCET w_i)

Architecture-specific

Case 2: System call

Where $w_d + w_c \leq w_0$

Decode (read only) (WCET w_d)

Commit (WCET w_c)

OS-specific (incl. *infoflow policies*)

Case 3: Domain switch

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Architecture-specific

Security proof approach

No channels!

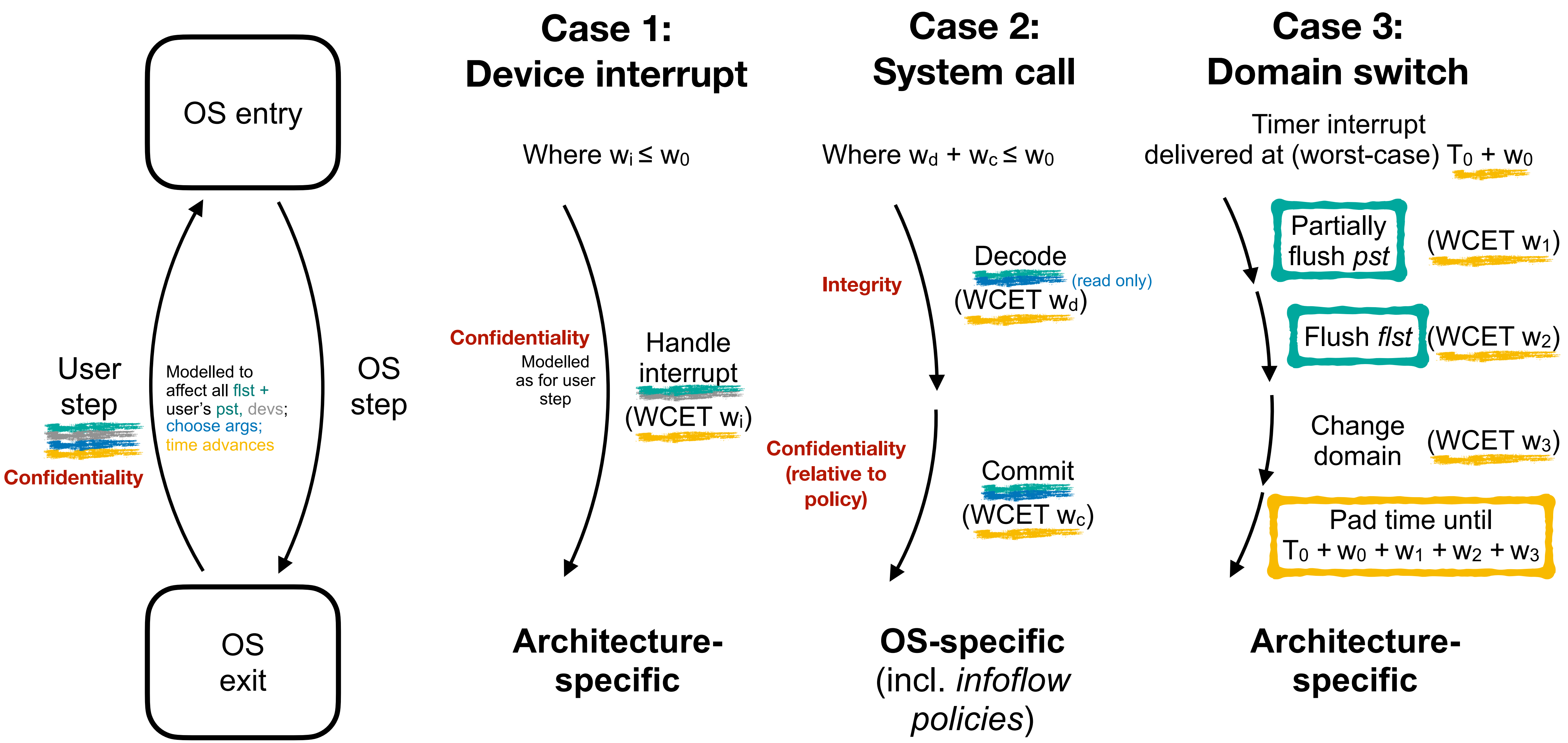
OS 🤝 HW

Microarchitecture
Devices
Policy-determining state
Time

Requirements

(In addition to WCETs)

Transition system



OS entry

User step

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Confidentiality

OS step

OS exit

Case 1: Device interrupt

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Confidentiality

Modelled as for user step

Handle interrupt (WCET w_i)

Architecture-specific

Case 2: System call

Where $w_d + w_c \leq w_0$

Integrity

Decode (read only) (WCET w_d)

Confidentiality (relative to policy)

Commit (WCET w_c)

OS-specific (incl. *infoflow policies*)

Case 3: Domain switch

Timer interrupt delivered at (worst-case) $T_0 + w_0$

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Pad time until $T_0 + w_0 + w_1 + w_2 + w_3$

Architecture-specific

Security proof approach

No channels!

OS 🤝 HW

Microarchitecture

Devices

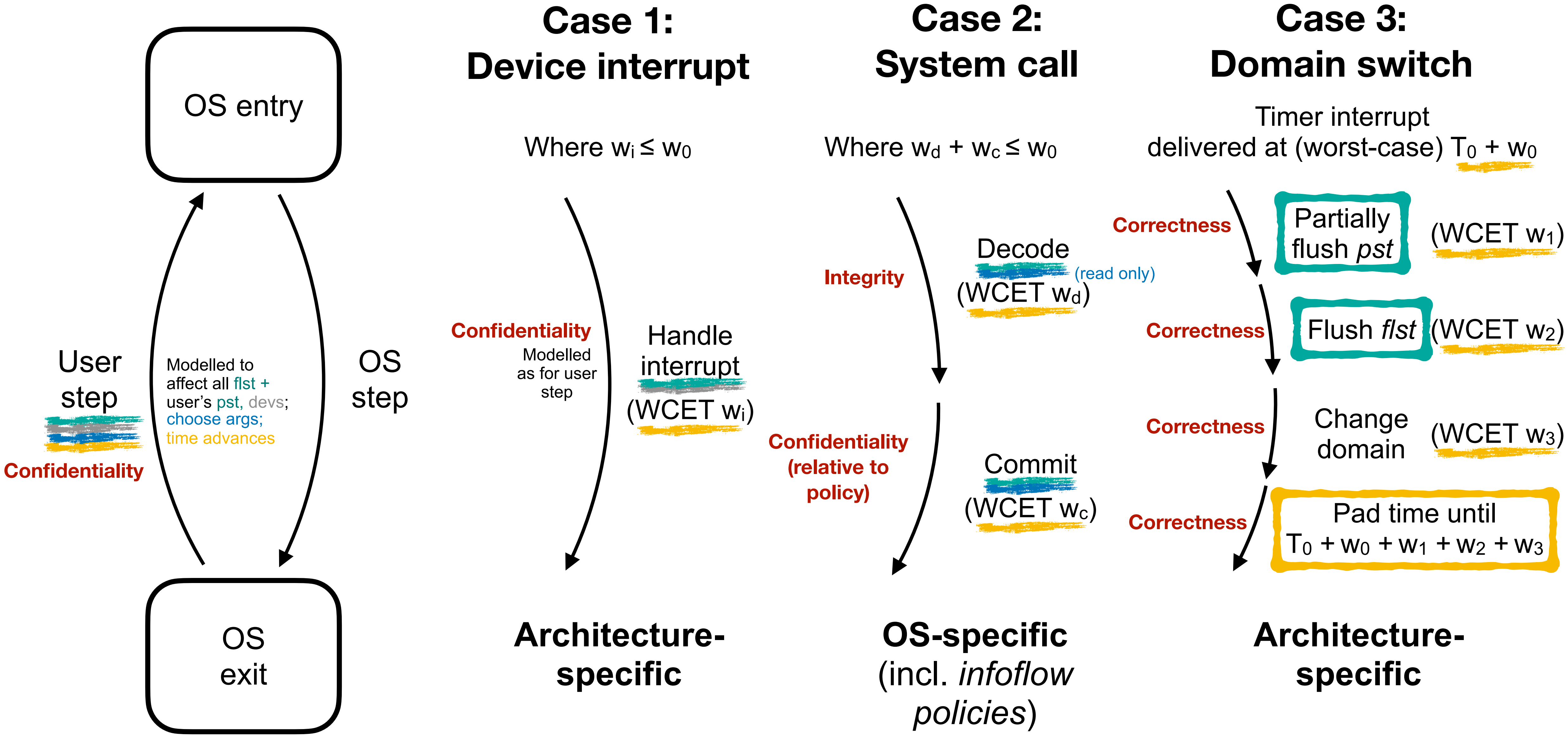
Policy-determining state

Time

Requirements

(In addition to WCETs)

Transition system



OS entry

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Confidentiality

OS step

OS exit

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Where $w_i \leq w_0$

Confidentiality

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Where $w_d + w_c \leq w_0$

Integrity

Decode (WCET w_d) (read only)

Confidentiality (relative to policy)

Commit (WCET w_c)

OS-specific (incl. *infoflow policies*)

Case 3: Domain switch

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Architecture-specific

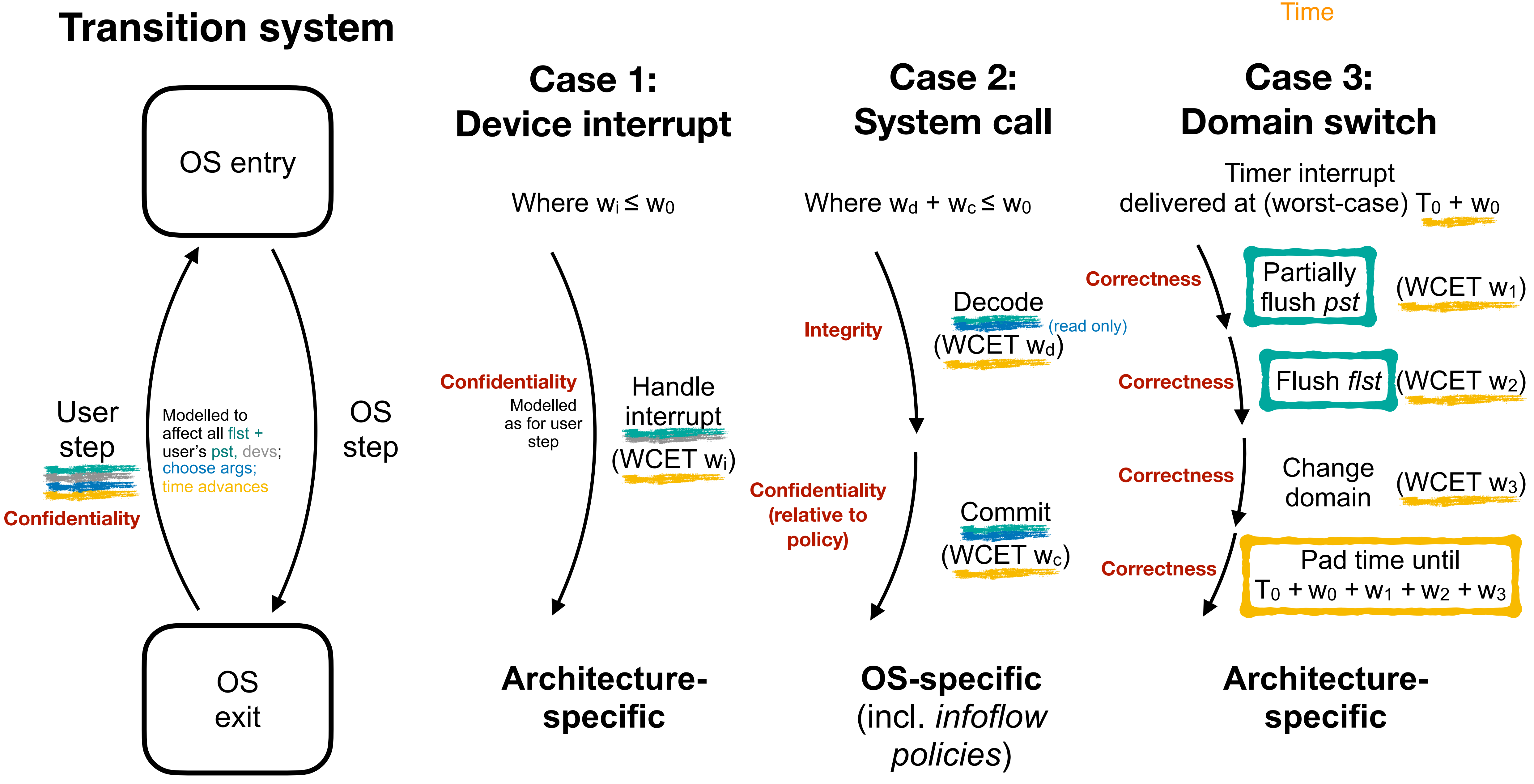
Security proof approach

No channels!

OS 🤝 HW

Microarchitecture
Devices
Policy-determining state
Time

Requirements
(In addition to WCETs)



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OS exit

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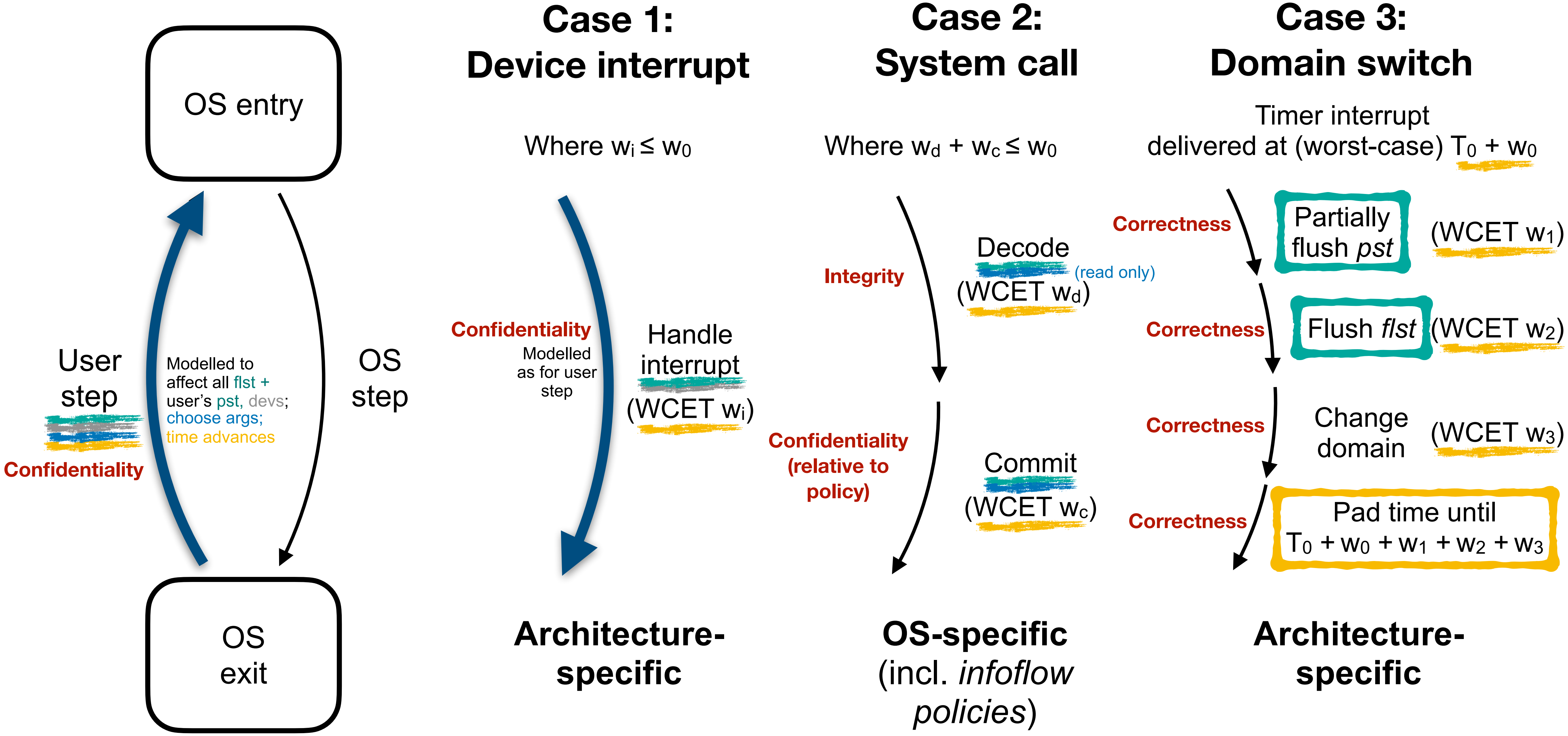

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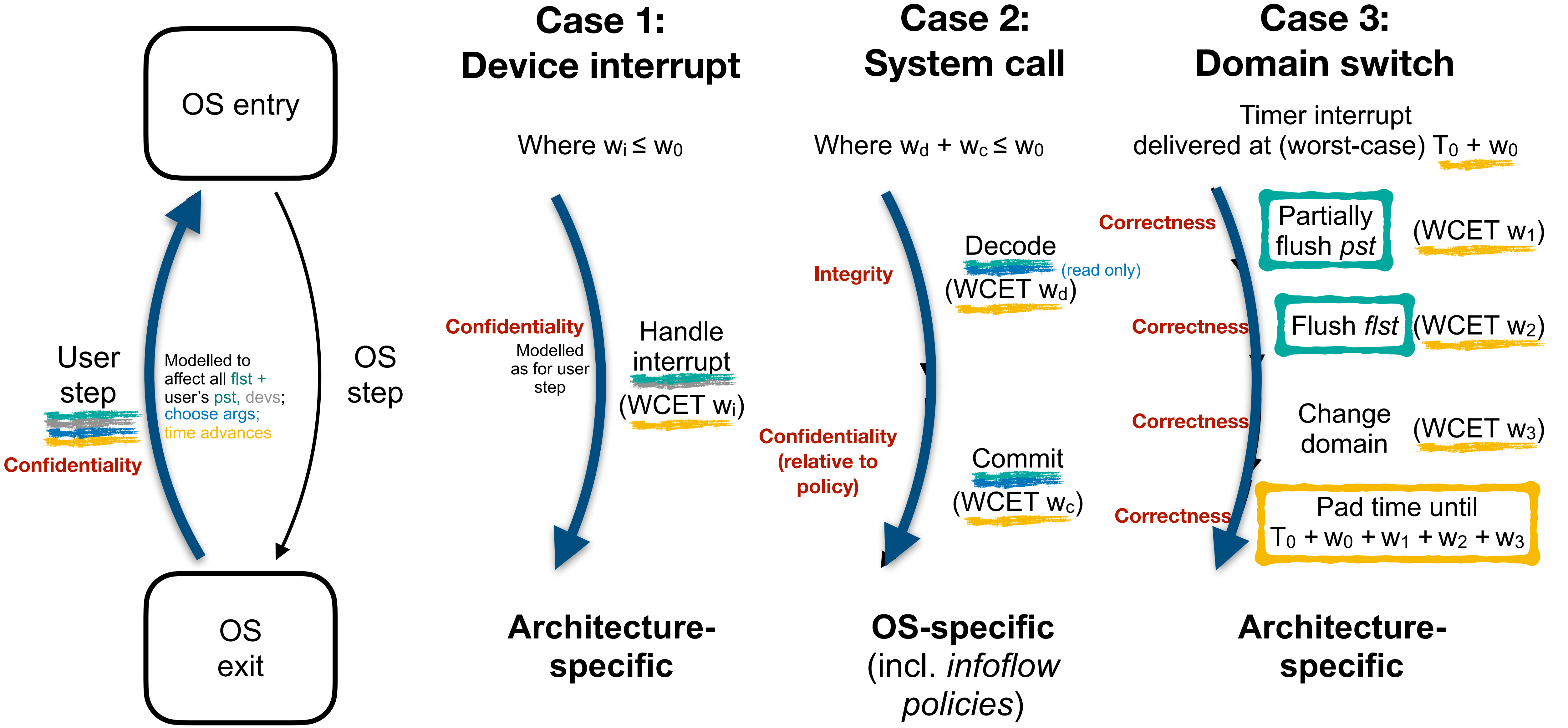

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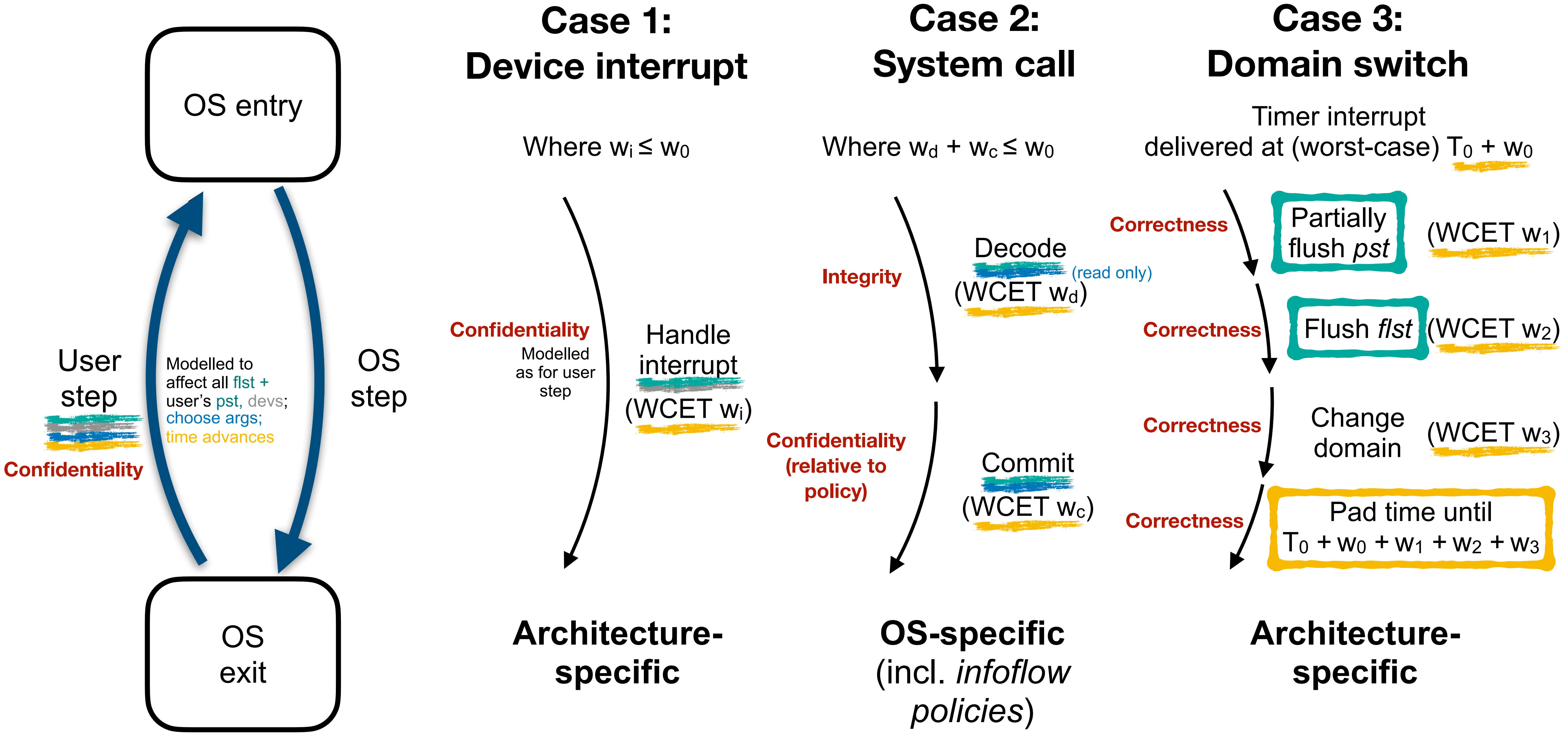

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How to formalise an OS enforces *time protection*?

Versus threat scenario:
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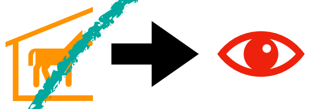

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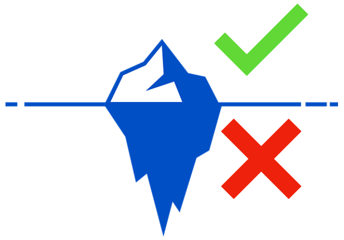

Make security property precise enough to exclude flows from covert state.

Demonstrating these principles,
we formalised in Isabelle/HOL:

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(Intended for seL4, but *generic*)

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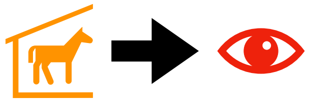

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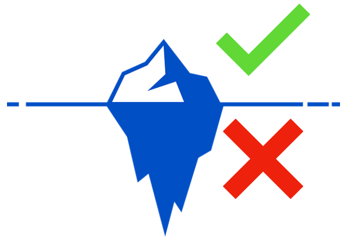

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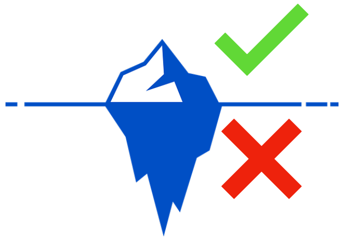

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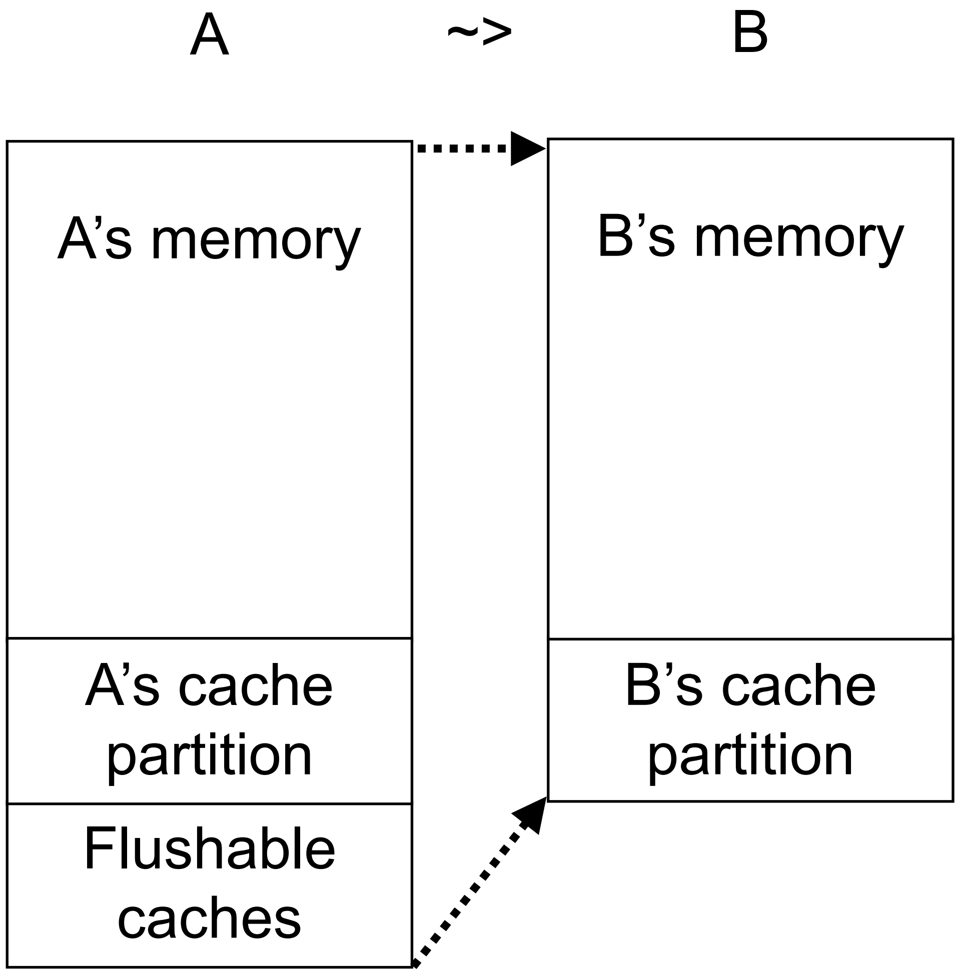
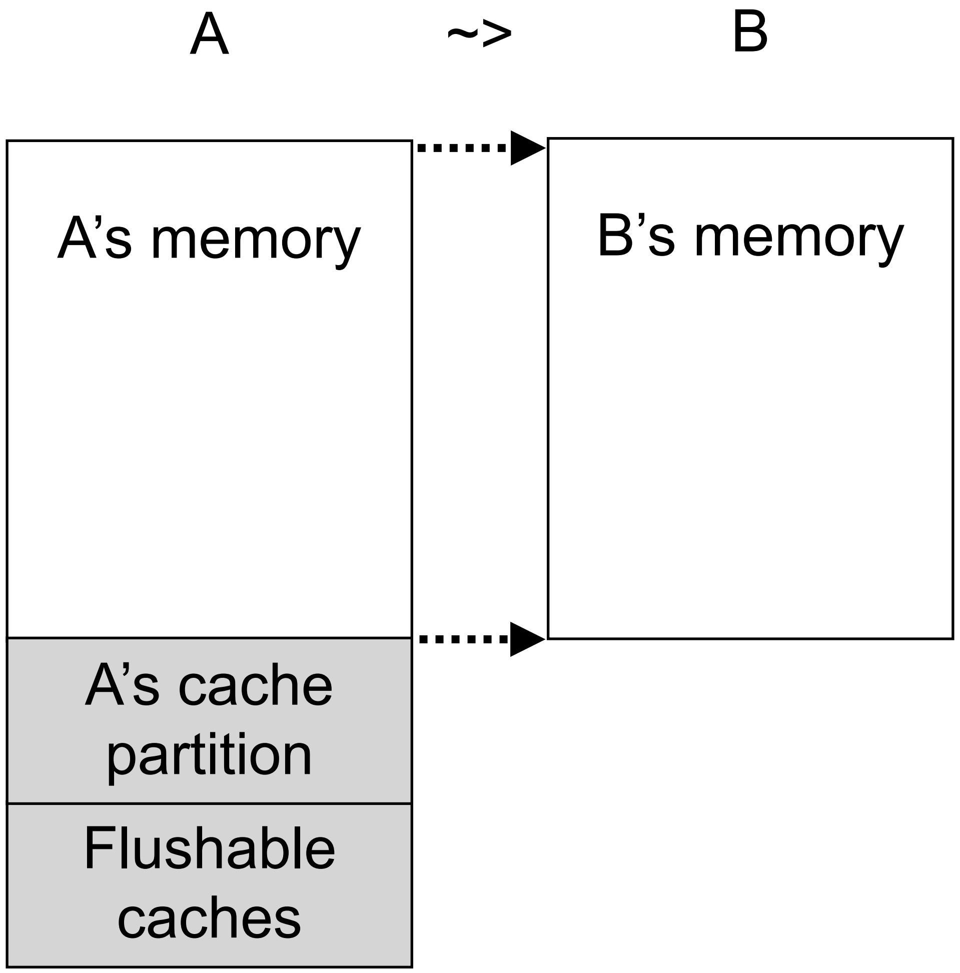


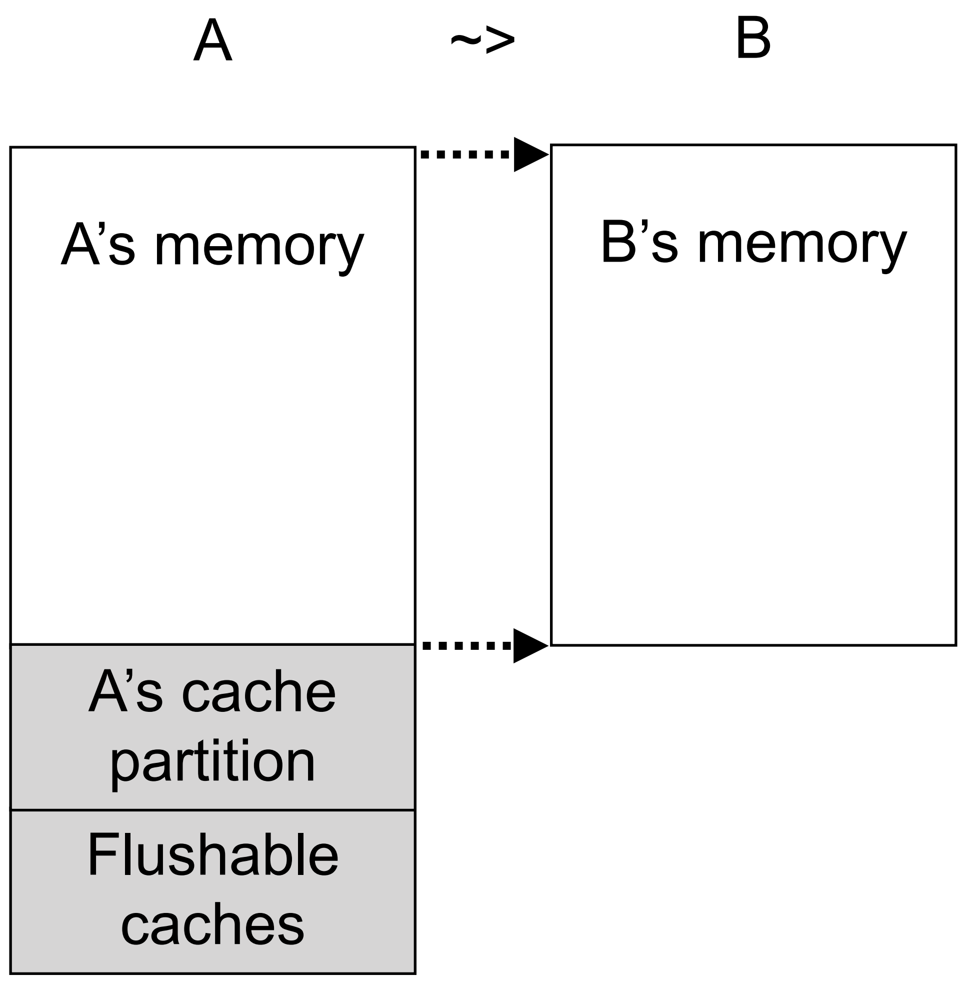


From prior seL4 infoflow proofs [Murray et al. 2012, 2013]: *"all or nothing" policies*

For time protection, need *spatial precision* to *allow some flows* but *exclude others*

OS security property

Our infoflow policies:



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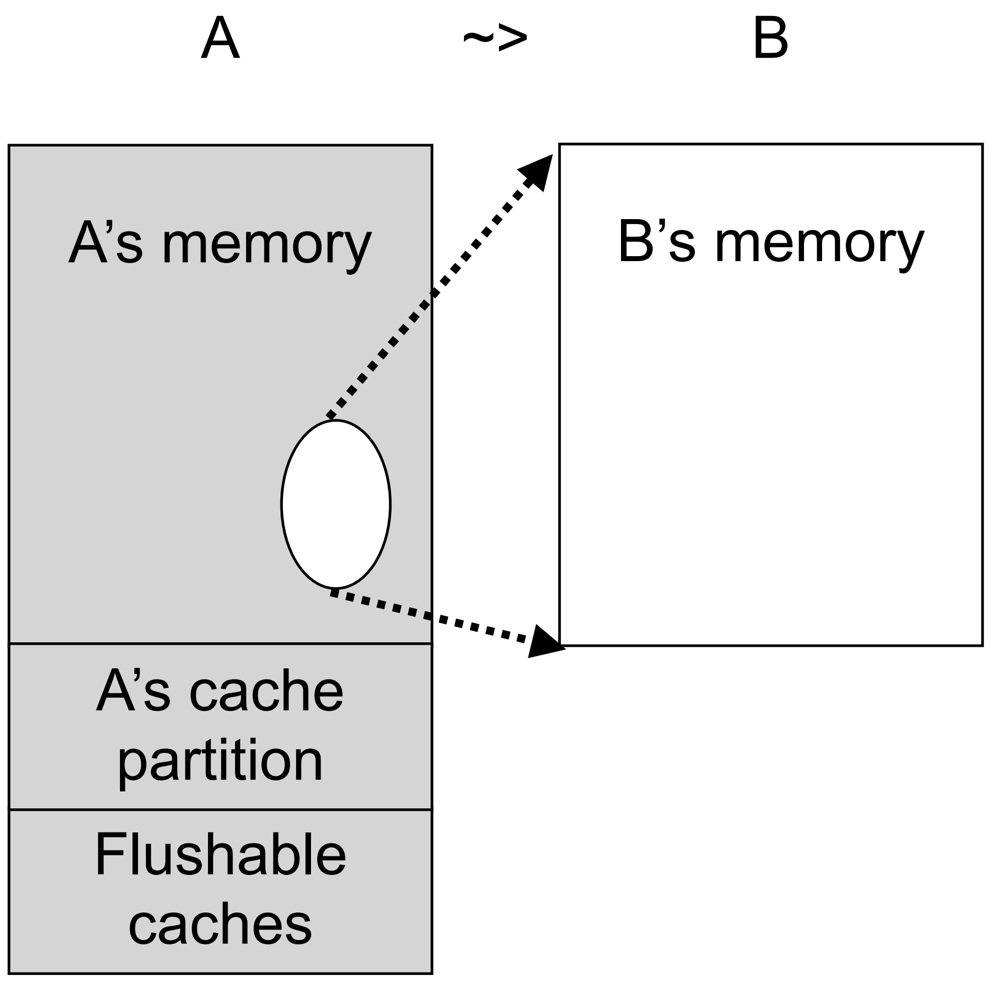

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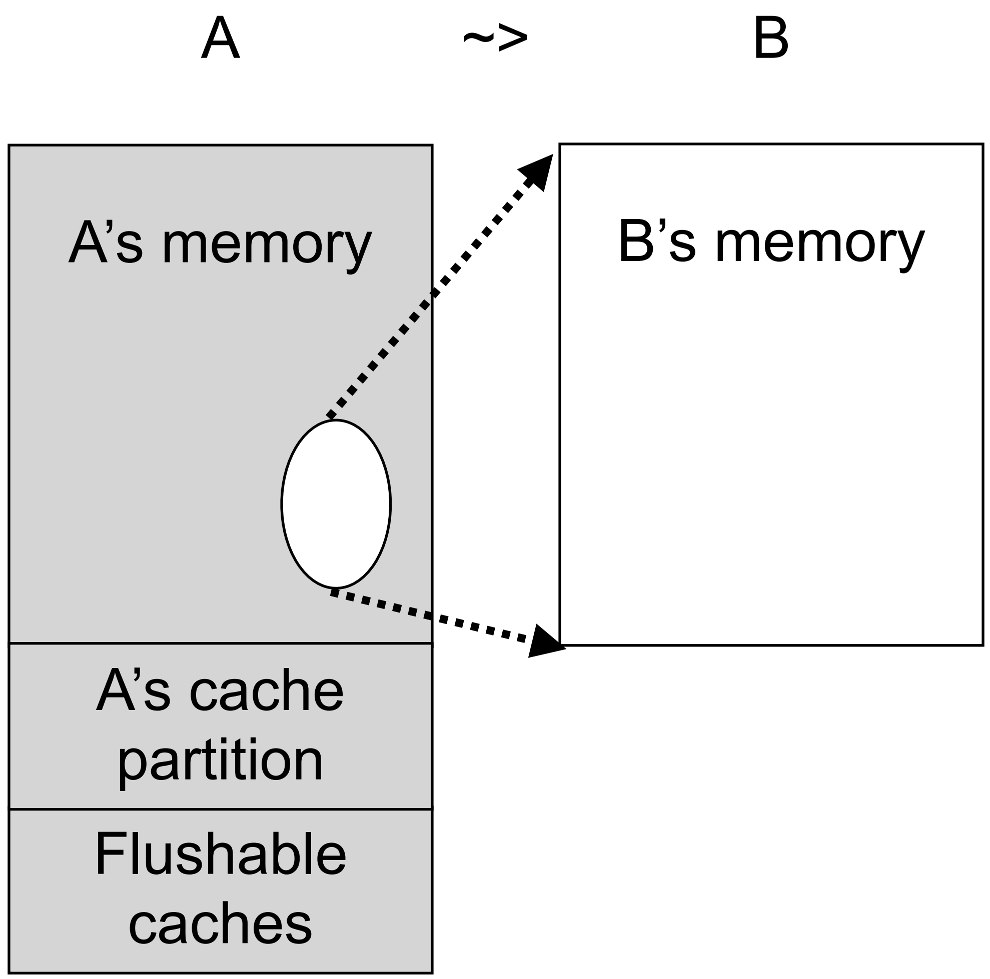

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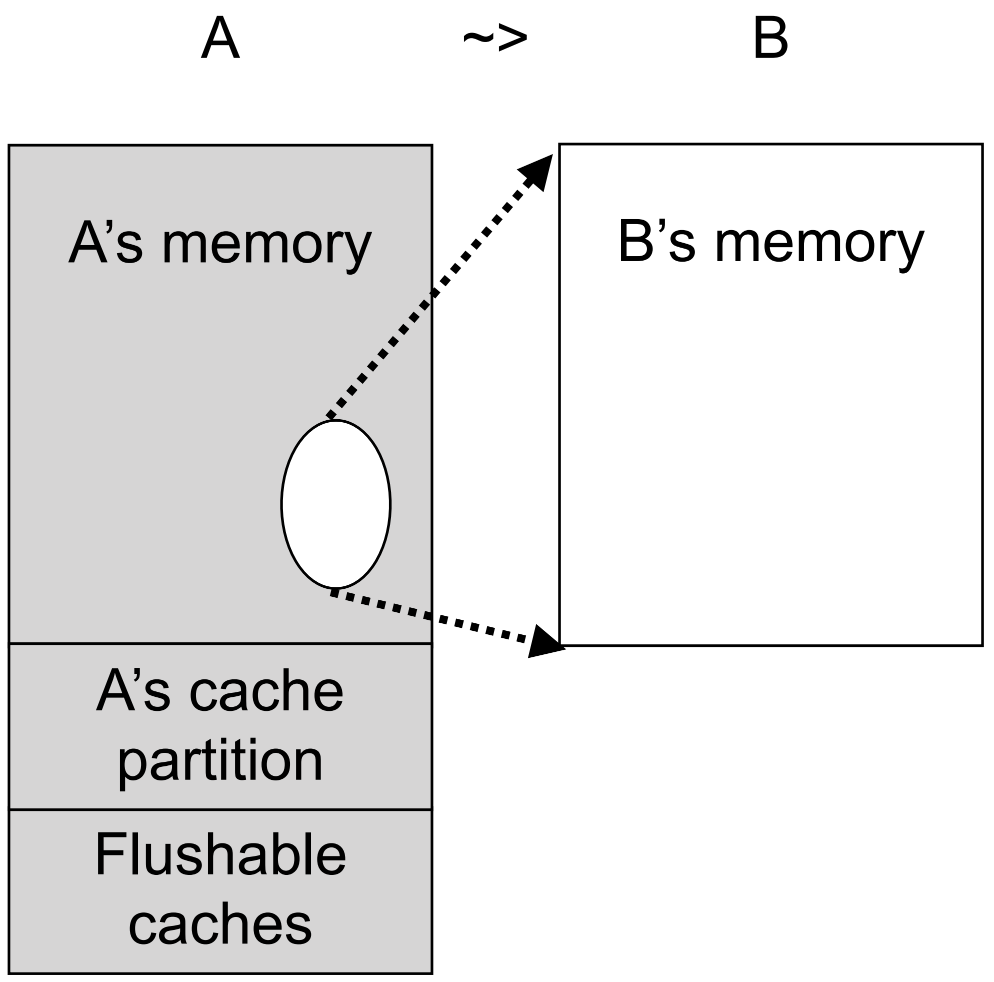
- Also arbitrary *temporal precision*



A ~> B

A's memory

B's memory

A's cache partition

Flushable caches

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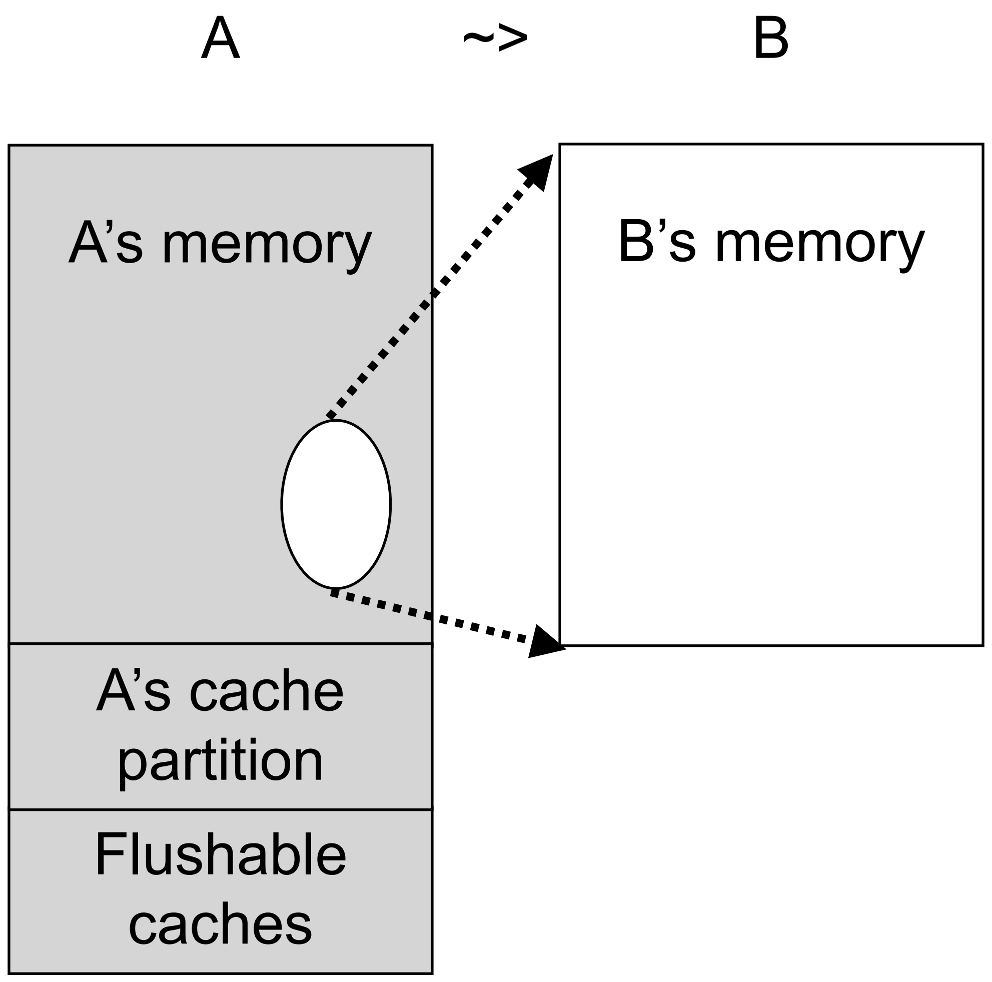

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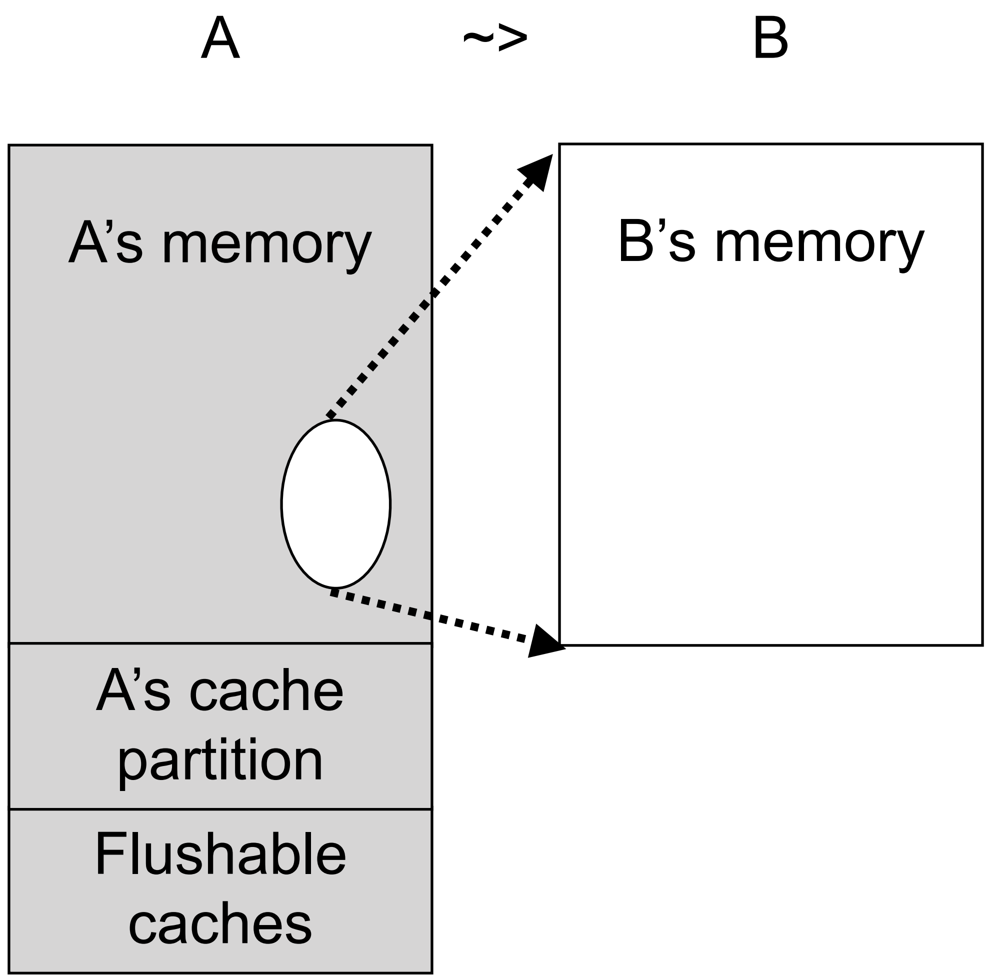

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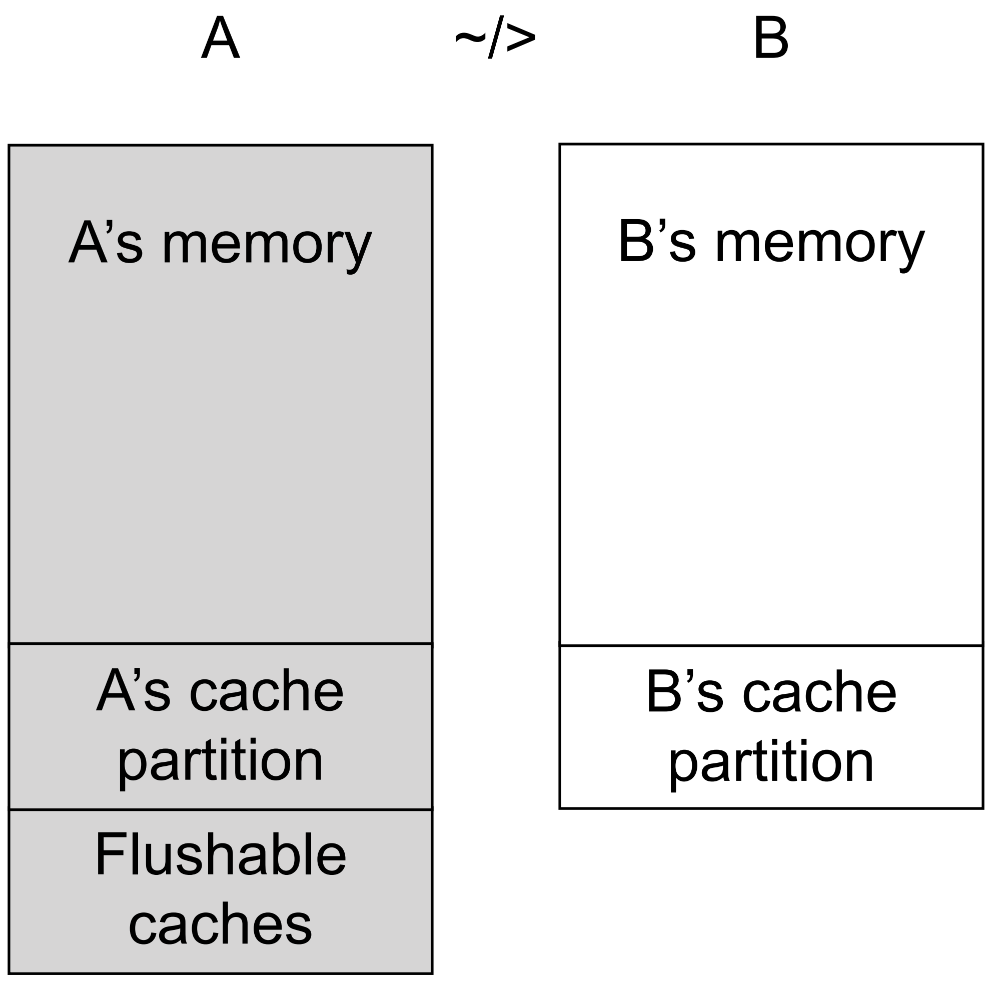
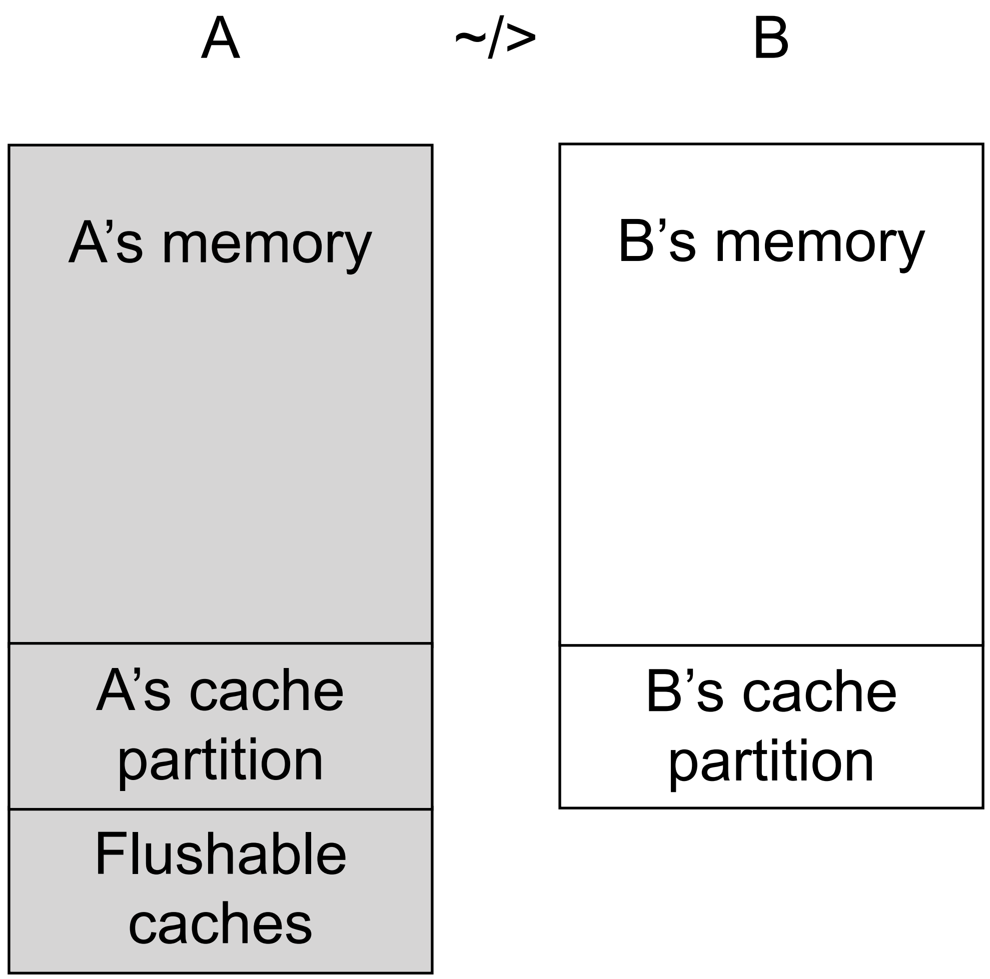


Dynamic policy, observer relativity

Two basic system calls:
Subscribe(*d*), Broadcast()



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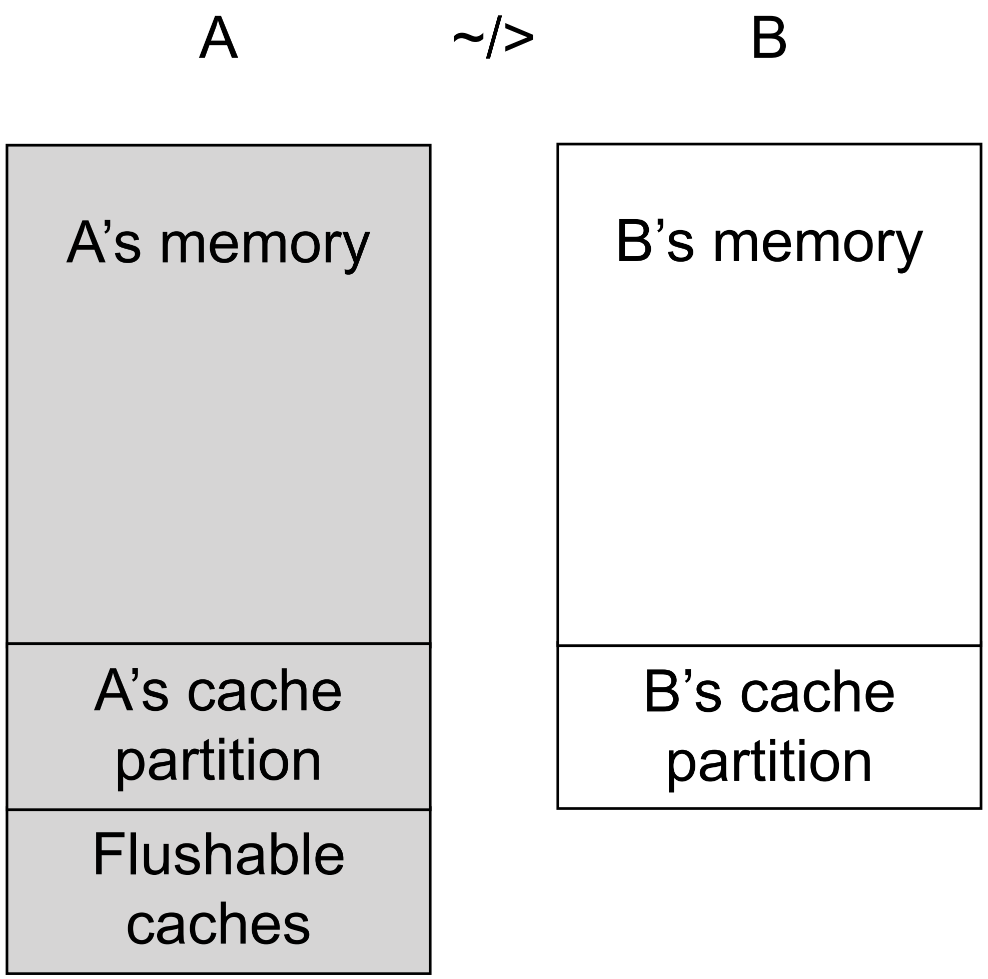

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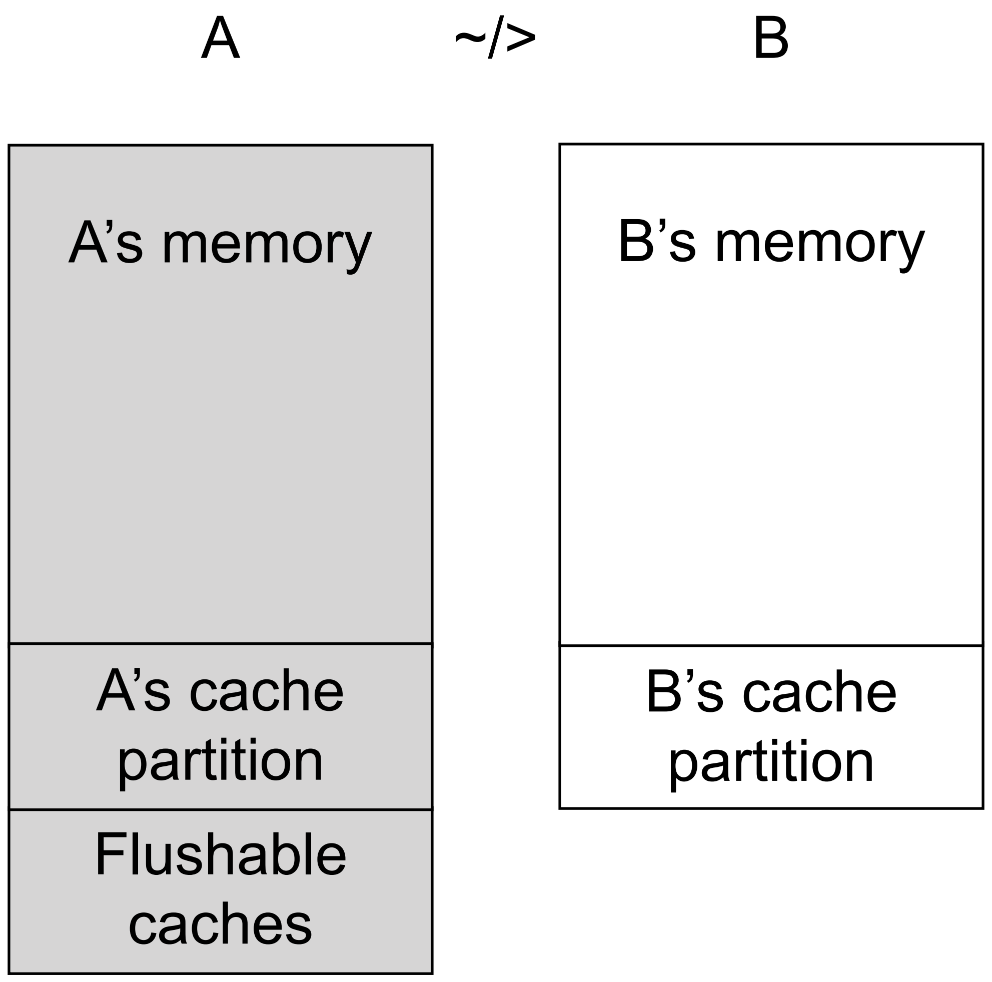

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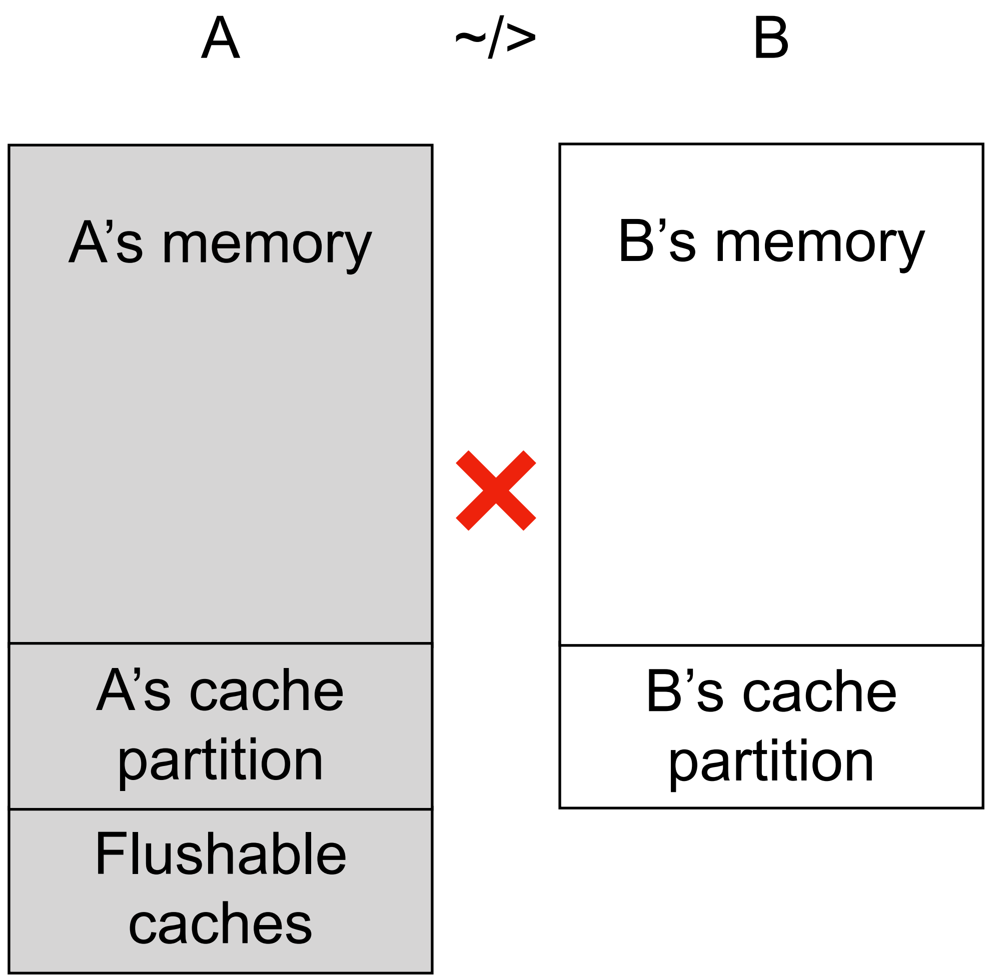

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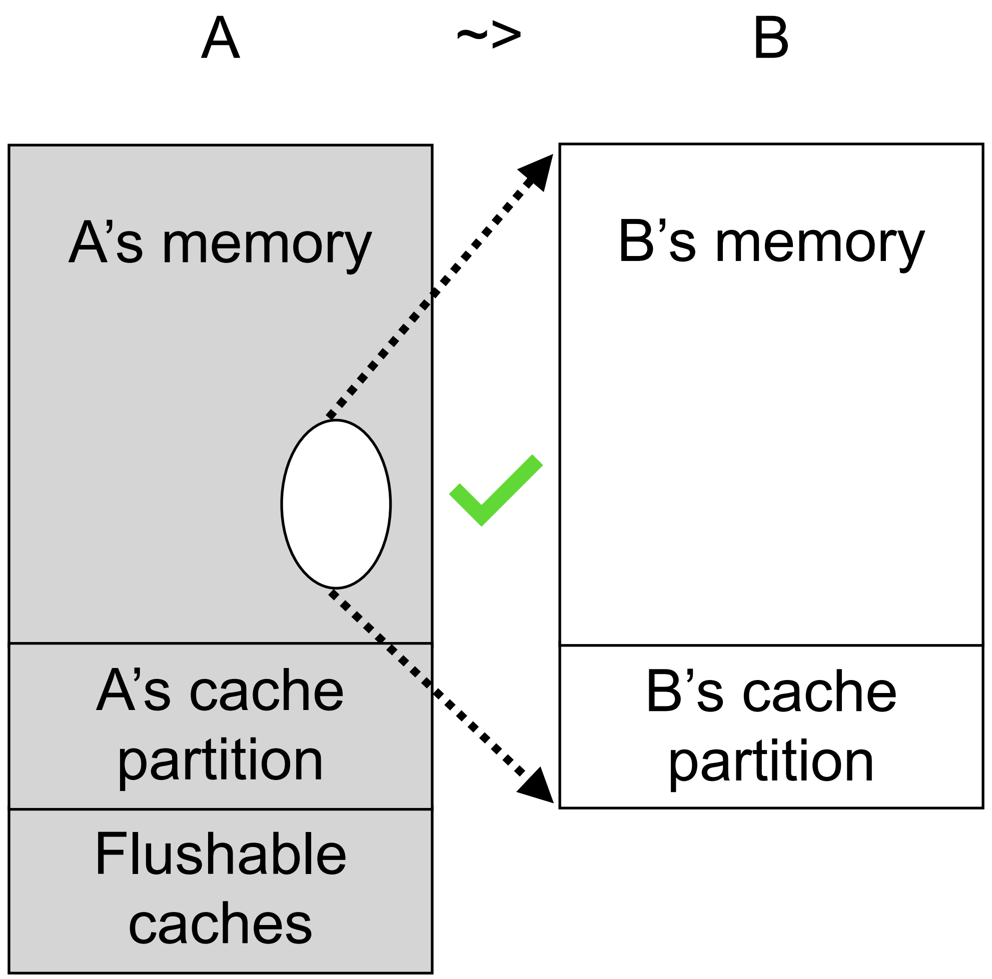

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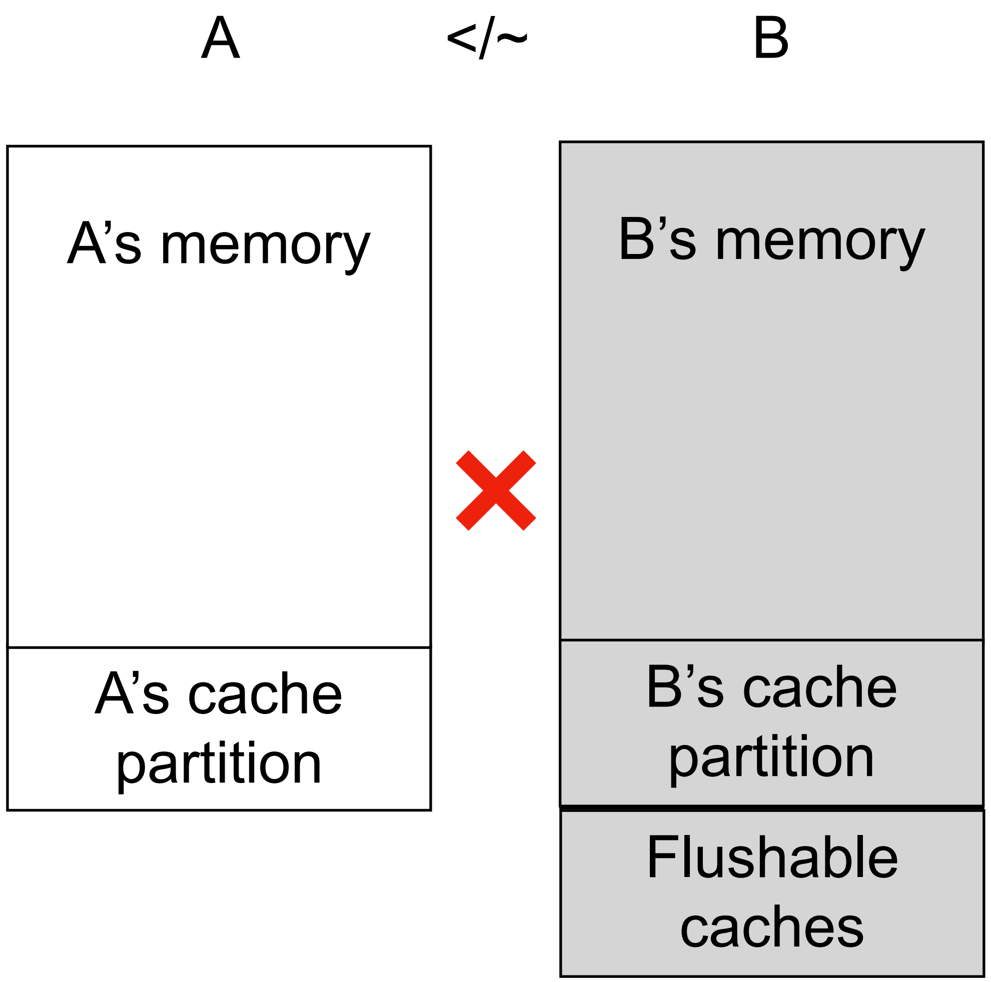

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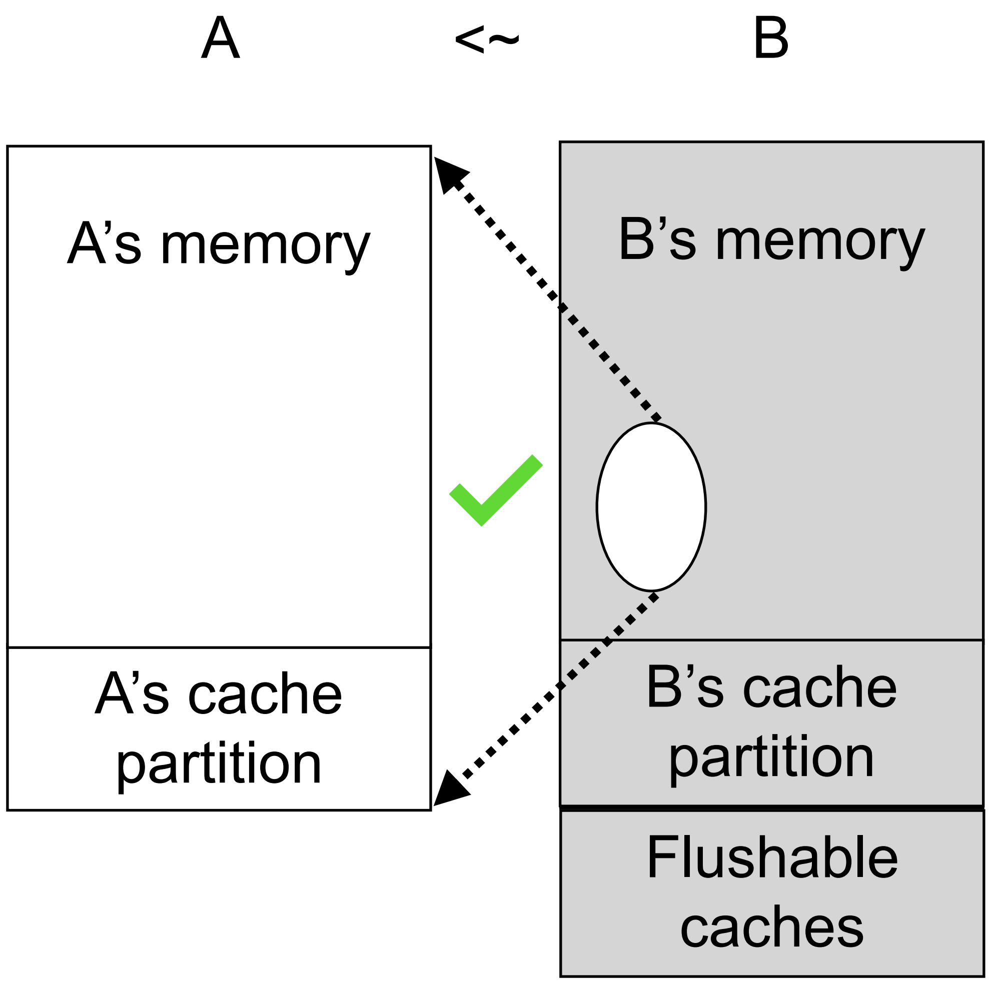

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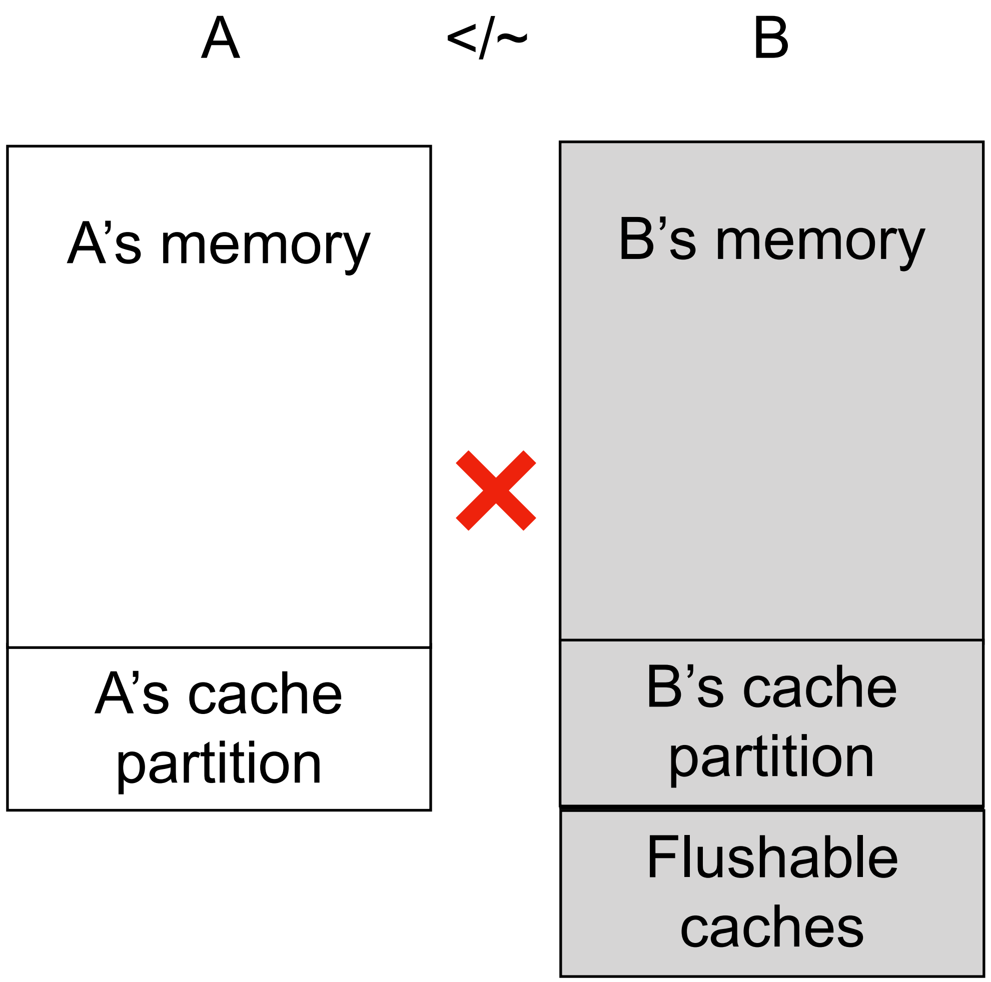

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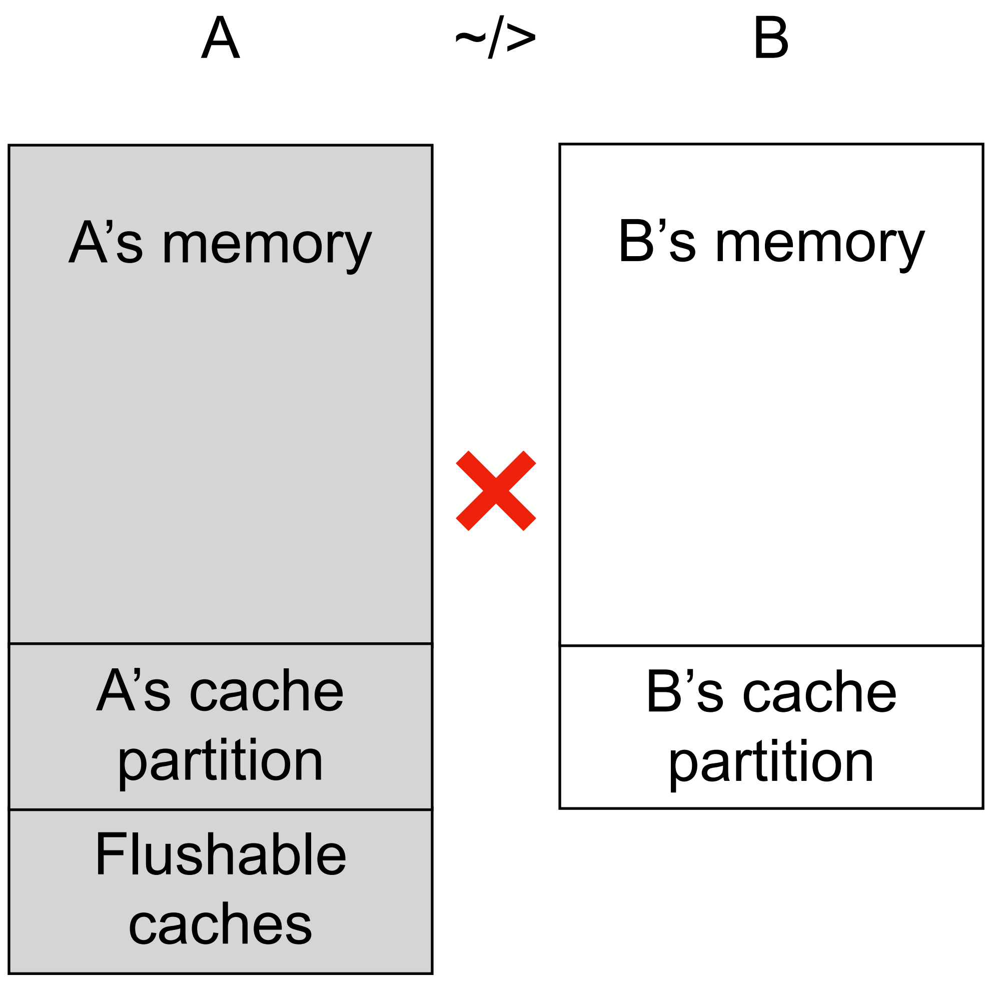

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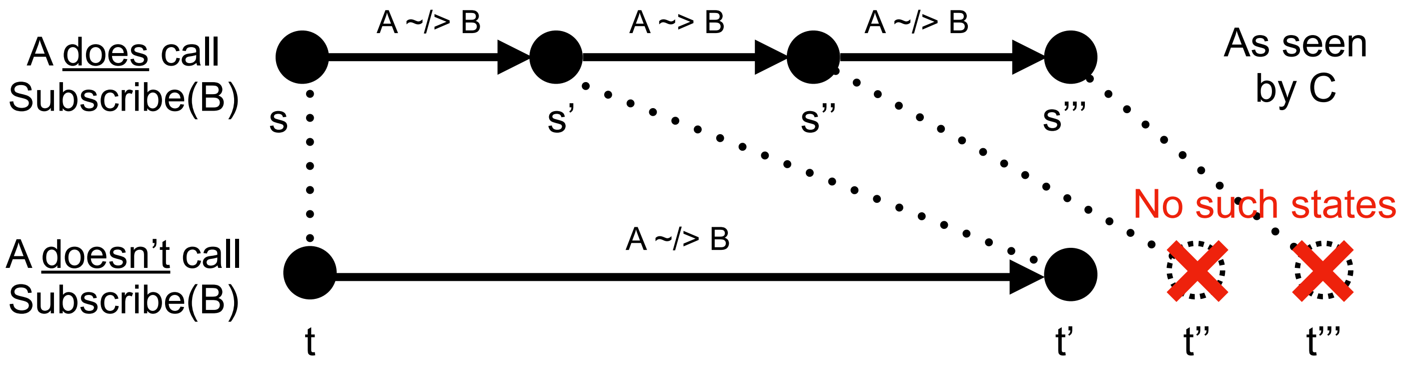

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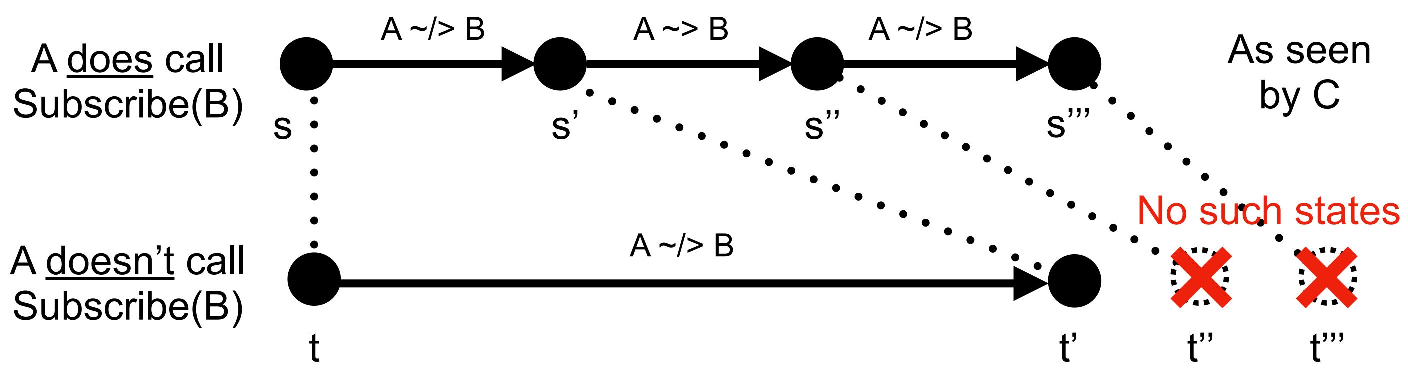

- *Solution*: C's property must treat *states* (in the state machine) as observable only whenever
  - C is running, or
  - When *d* is running, *d* ~> C.

How to formalise an OS enforces *time protection*?

Versus threat scenario:
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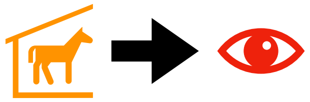

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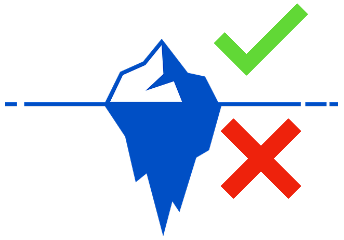

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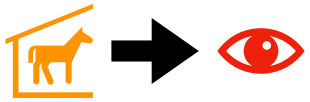

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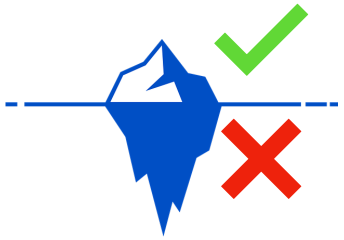

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Thank you!
Q & A

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Paper: https://doi.org/jzwj
Artifact: https://doi.org/jzwk

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